

# Story of Pinned Photodiode and Sony HAD Sensor

Sony Kumamoto Technology Center is the center of Image Sensor World.



Hagiwara visited his friends in Sony Kumamoto Technology Center on November 19, 2018.

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Hagiwara explained why Sony is now so strong in the Image Sensor World.

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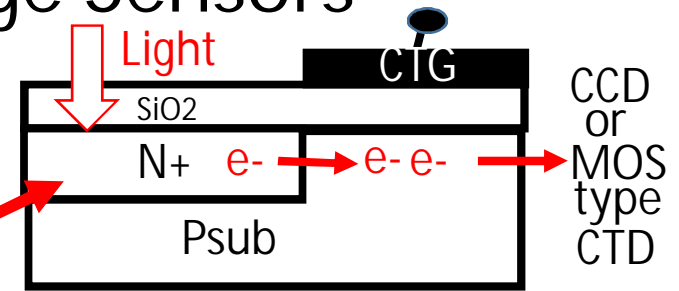
The reason why Sony is so strong in the Image Sensor World.

- (1) Ibuka dreamed of the important application of the bipolar transistor technology.
- (2) Kawana and Kato made important contributions to improve Sony bipolar transistor technology.
- (3) Iwama dreamed of the important application of the charge transfer device (CCD) technology.
- (4) Hagiwara had an idea to create a super sensitive low-noise and image-lag free photodiode.
- (5) Many Sony process engineers, including Suzuki, Ueda and Shimizu, work together diligently to create Sony semiconductor process and device technology.

Hagiwara photodiode is now called as either SONY HAD Sensor , Pinned Photodiode or Buried Photodiode. The photo signal charge stored in this photodiode is transferred to the adjacent charge transfer device (CTD) in the complete depletion mode. The charge transfer device (CTD) can be either a CCD type CTD or a CMOS type CTD. That is, the charge coupled device type charge transfer device (CCD CTD) or the modern CMOS type charge transfer device ( CMOS CTD ). We all know now that the CMOS CTD is much better.

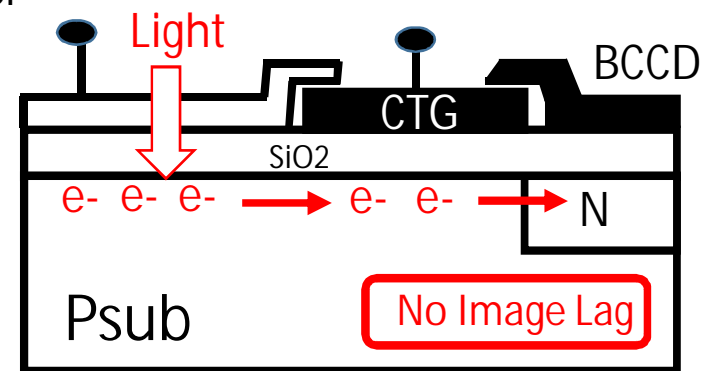
# Early Developments of Image Sensors

Both Classic MOS image sensor and Classical ITL CCD image sensors with the heavily doped N+ diffusion type (N+P junction) photodiode had a serious image-lag problems. Blue light sensitivity was OK. **Bad Image Lag**

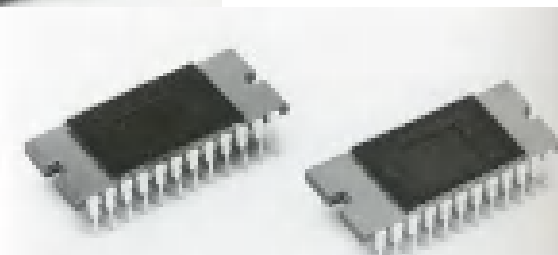


## Transparent Electrode MOS Capacitor Photodiode with SCCD type CTG and BCCD type CTD

Sony developed an image-lag free ILT CCD image sensor with a transparent electrode MOS capacitor type photodiode with the CCD complete charge transfer of the image lag free feature. And the two chip CCD video camera was installed in the cockpit of the Jumbo 747 in 1980. But it still had a serious surface dark current and the surface trap noise problems.



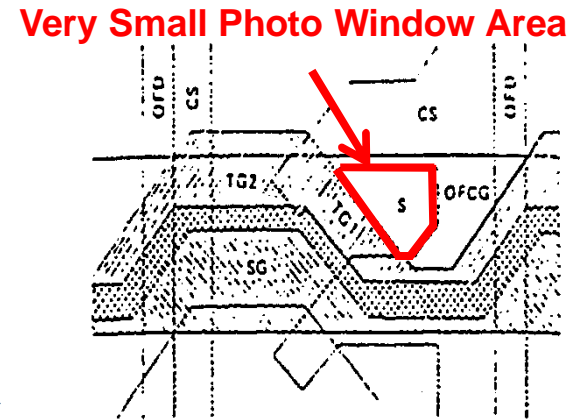
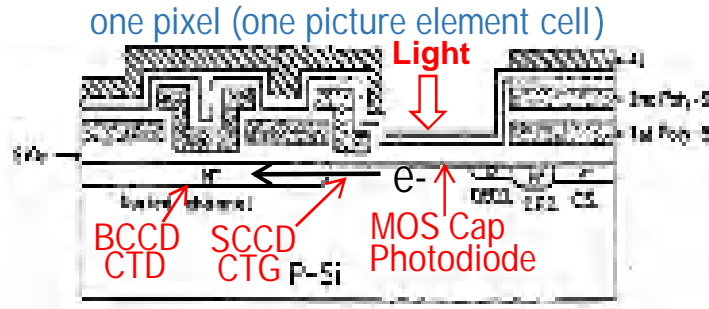
Sony XC-1 1980  
Two-Chip CCD  
Color Video Camera



Sony ICX-008 CCD chips

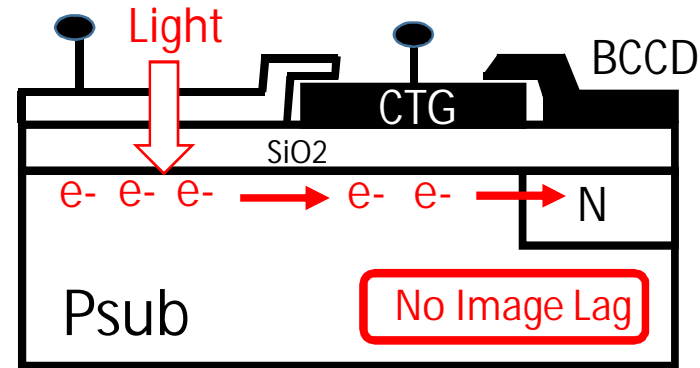
「高密度インターライン転送方式CCD撮像素子」  
岡田静夫、島田孝、松本博行、安藤哲雄、狩野靖夫、桑沢哲郎、萩原良昭  
Japan SSD Conference, DDD78-5, May, 1978.

Serious surface dark current was still the big head ache.



Hagiwara thought the surface trap noise can be quenched by applying the buried channel CCD type MOS photodiode.

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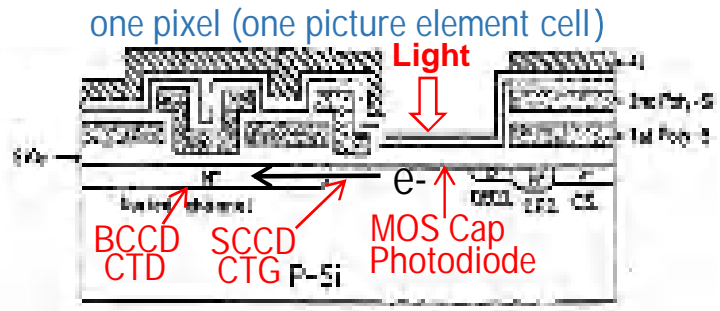
Sony XC-1 1980 Two-Chip CCD Color Video Camera



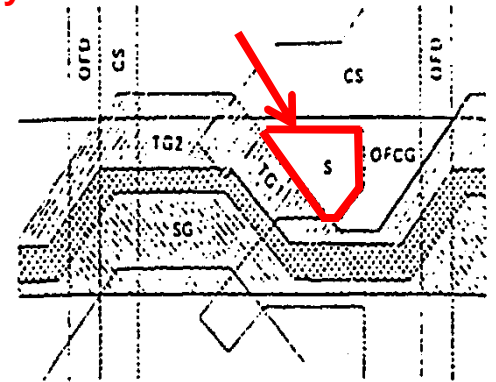
Sony ICX-008 CCD chips

「高密度インターライン転送方式CCD撮像素子」  
 岡田静夫、島田孝、松本博行、安藤哲雄、狩野靖夫、桑沢哲郎、萩原良昭  
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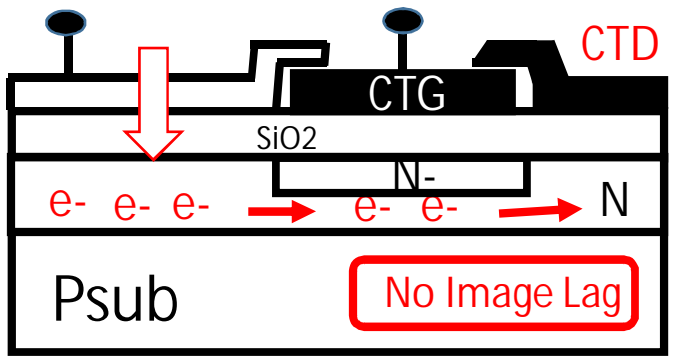
Serious surface dark current was still the big head ache.



Very Small Photo Window Area



to save pixel area, the vertical Overflow Drain (VOD) was desired.



Hagiwara thought the surface trap noise can be quenched by applying the buried channel CCD type MOS photodiode. The lightly doped buried channel type N diffusion (NP junction) photodiode can operate as the BCCD type complete charge transfer mode without image lag and trap noise. But it still had a serious surface dark current due to the strong surface electric field of the BCCD type MOS capacitor photodiode, together with the bad surface positive fixed charge +Q<sub>ss</sub>.

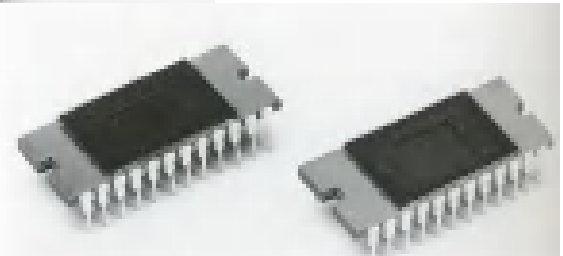


ANA 747 Jumbo Jet with SONY CCD camera

No Image Lag



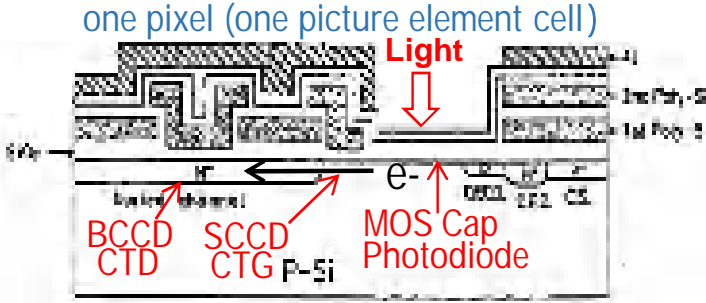
Sony XC-1 1980 Two-Chip CCD Color Video Camera



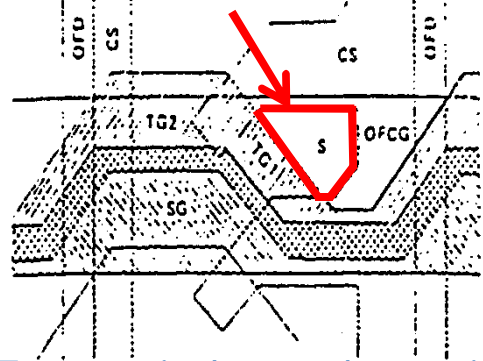
Sony ICX-008 CCD chips

狩野、安藤、松本、萩原、橋本、"インターライン転送方式 CCD撮像素子" テレビジョン学会、電子装置研究会 ED 481, pp.47-52, Jan 24, 1980.

Serious surface dark current was still the big head ache.



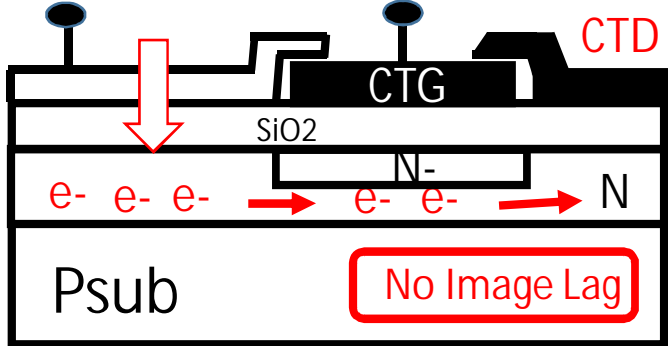
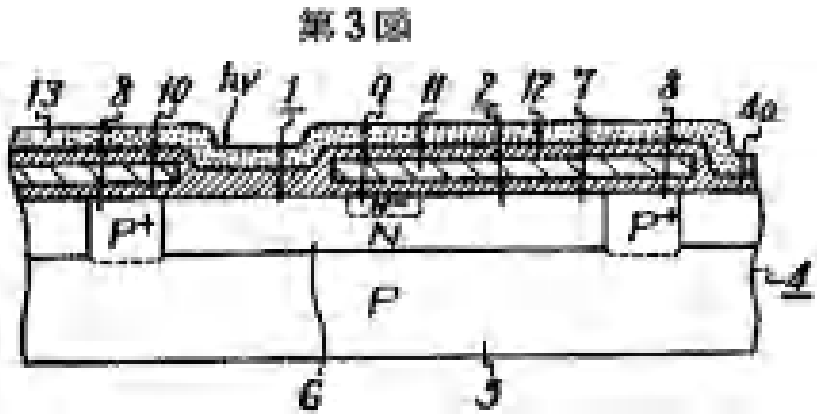
Very Small Photo Window Area



To save pixel area, the vertical Overflow Drain (VOD) was desired.

Hagiwara thought the surface trap noise can be quenched by applying the buried channel CCD type MOS photodiode.

Hagiwara now had the idea to solve these two problems, and filed a Japanese patent 1975-134985 in Nov 13, 1975.



Hagiwara drew the ILT CCD type transparent electrode MOS capacitor photodiode as the conventional structure in the Fig. 3 of the Hagiwara 1975 Patent as shown above.

Hagiwara understood the conventional SiO2 exposed heavily doped N+P photodiode has a good blue light sensitivity. Hagiwara wanted to keep the buried channel type lightly doped N diffusion NP junction type photodiode for the BCCD type complete charge transfer mode operation for keeping the image lag free picture quality. But the surface electric field causing the serious dark current was still the headache.



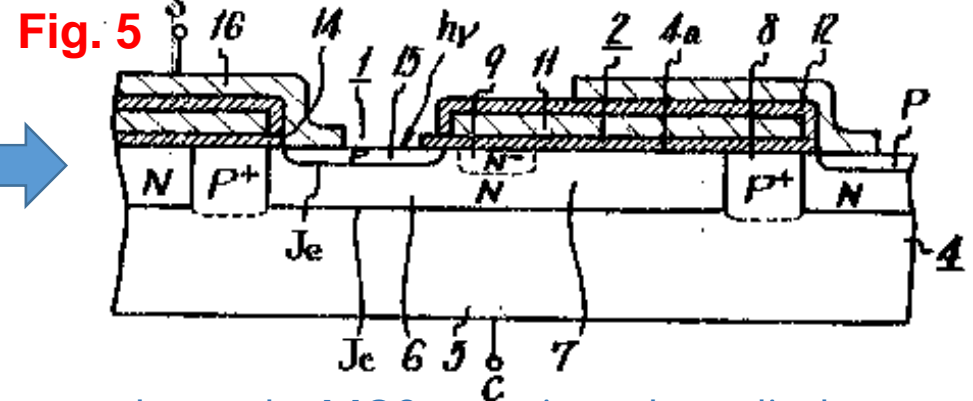
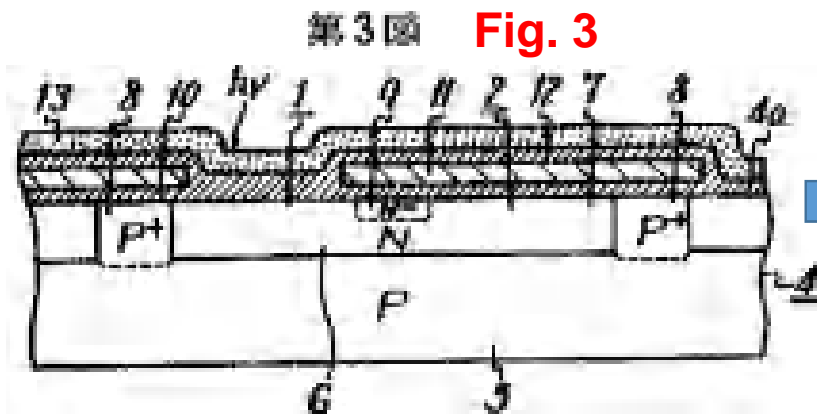
Serious surface dark current was still the big head ache.

Hagiwara thought that the surface dark current and the bad surface positive fixed charge  $+Q_{ss}$  can be quenched by the shallow but highly dosed implantation of boron  $P^+$  ions to create the highly doped  $P^+$  diffusion of surface hole accumulation layer. The result is the Pinned Photodiode with the pinned window with the Pinned surface potential.

Hagiwara thought the surface trap noise can be quenched by applying the buried channel CCD type MOS photodiode.

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The metal contact to the  $P^+$  surface hole accumulation layer is optional as one of many variety of application examples of VOD function modes.



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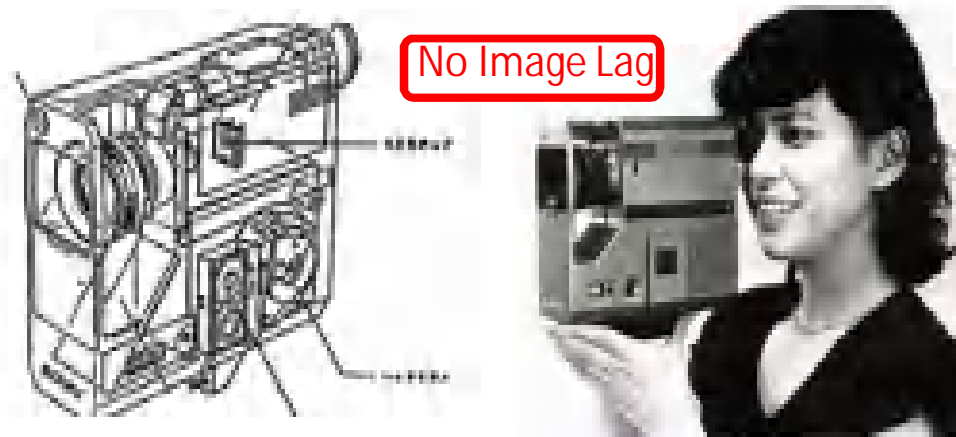
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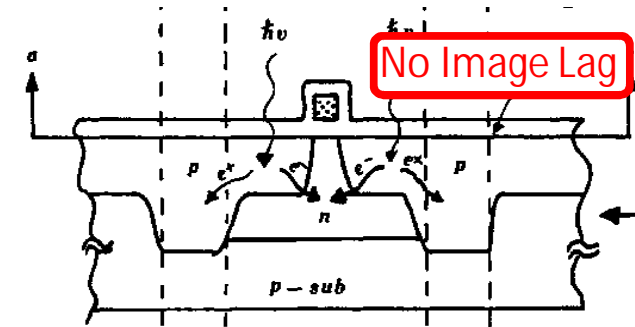
SONY HAD ( Pinned Photodiode ) Original Technical Publication in 1979  
and the Tokyo and New York Press Conference in 1980

The original Pinned Photodiode (PPD) structure was invented by Hagiwara at Sony in 1975. The first one-chip color video camera with a FT CCD image sensor with PNP junction type Pinned Photodiode (PPD) was reported by Sony in 1980 at Tokyo Press Conference by Iwama Kazuo of Sony president, and at New York Press conference by Morita Akio of Sony chairman.

Sony original 570H x 498 V one-chip FT CCD Image Sensor with Pinned Photodiode, July 1980



The P+NP Junction Pinned Photodiode 1978



On July 1980, Iwama Kazuo at Sony Tokyo Press Conference and Morita Akio at New York Press Conference announced the one chip CCD video camera with the 8 mm VTR in one box.

**See the Original 1978 Publication of the Pinned Photodiode Sensor**

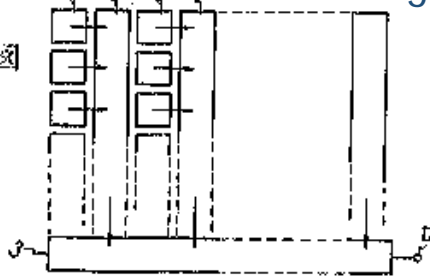
Y. Daimon-Hagiwara, M. Abe, and C. Okada, "A 380Hx488V CCD imager with narrow channel transfer gates," Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Applied Physics, vol. 18, supplement 18-1, pp. 335-340, 1979

High quality picture of SONY CMOS Image is also based on SONY HAD ( Pinned Photodiode).

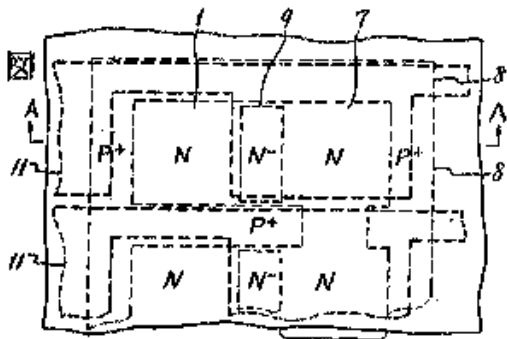
# Pinned Photodiode(P+NP) and Sony HAD (P+NP/Nsub) are identical.

Interline Transfer CCD image sensor

第 1 圖

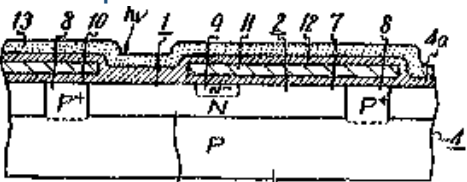


第 2 圖



Conventional Image Lag Free CCD type MOS Capacitor Photodiode

第 3 圖



Japanese Patent 1975-134985

P+NP junction type PPD with Pinned P+ surface

第 5 圖  
Fig.5

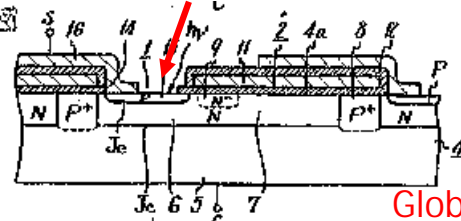


Fig.5 shows Image Lag Free P+NP junction type Pinned Photodiode

第 6 圖

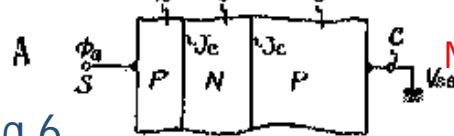
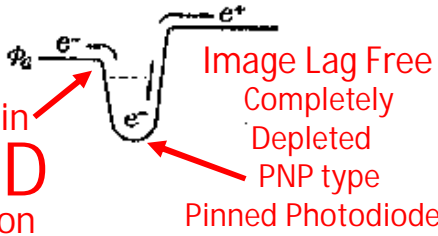


Fig.6

Built-in VOD function



Japanese Patent 1975-127647

第 7 圖

Pinned N+ surface

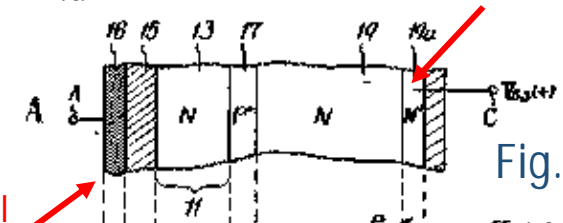


Fig.7

Global Shutter One Time MOS Gate Capacitor Buffer Memory

No Dark Current

Completely Depleted N+NP junction Image Lag Free Pinned Photodiode

Fig. 7 shows Image Lag Free N+NP+N junction type Pinned Photodiode

Hagiwara Yoshiaki thinks that Hagiwara invented the Pinned Photodiode in 1975. Hagiwara Yoshiaki thinks that Hagiwara is the inventor of the Pinned Photodiode. Hagiwara is now trying to ask the Japanese Patent Office to acknowledge his 1975 inventions. If you agree with Hagiwara, please support him one way or another.

The P+NP transistor operation modes include the two diode dynamic operation modes. The Pinned Photodiode (SONY HAD) operation is also a dynamic phototransistor operation.

Transistor operation modes include the operation modes of two diodes (  $J_e$  and  $J_c$  ).

### Two Operation Modes of PN junction ( diode )

- (1) Forward Bias Mode
- (2) Reverse Bias Mode

### Four Operation Modes of PNP junction ( transistor )

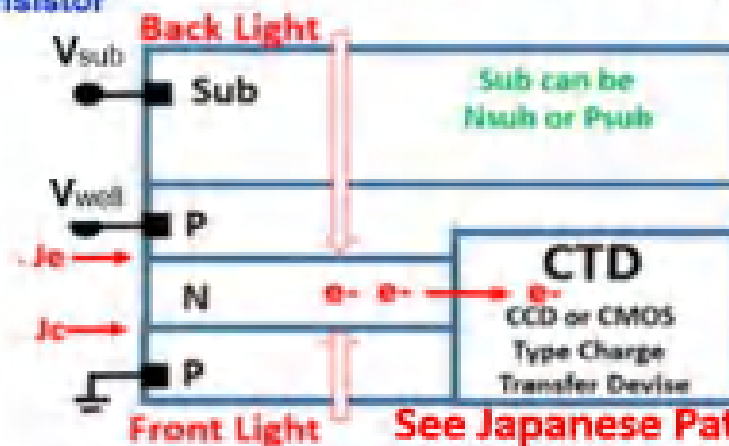
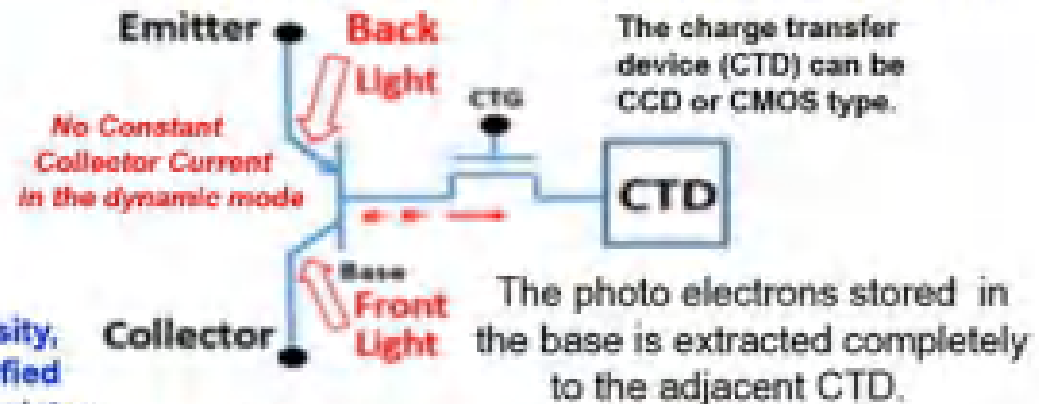
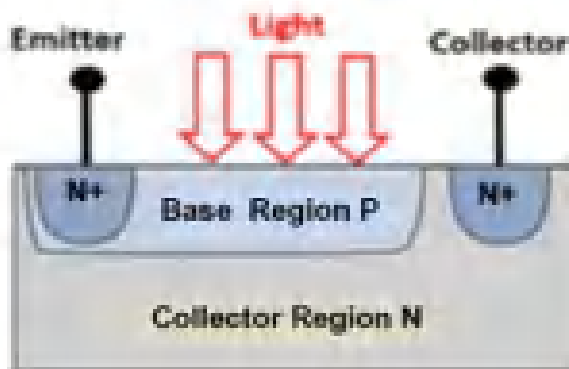
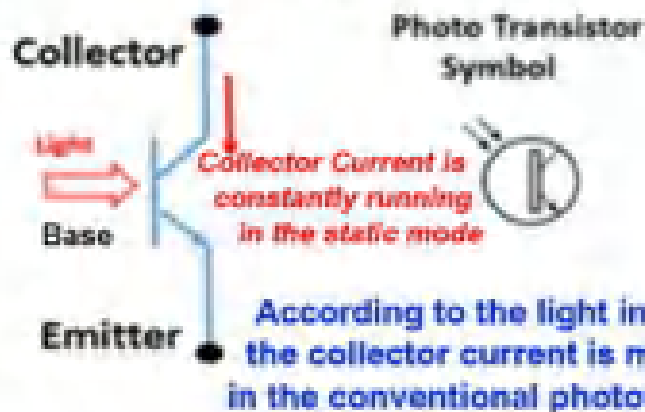
$J_c$ \ $J_e$	Forward Bias	Reverse Bias
Forward Bias	Large Current Burn-out Mode	Reverse Current Amplification Mode
Reverse Bias	Normal Current Amplification Mode	Dynamic Floating Capacitor Mode <b>Pinned Photodiode Mode</b> <b>Sony HAD Sensor</b>

$J_c$  = Collector Junction

$J_e$  = Emitter Junction

The P+NPsub junction type Pinned Photodiode with the Vertical Overflow Drain (VOD) was invented by Hagiwara at Sony in 1975, developed finally in the complete form in 1984 and named as Sony original HAD sensor. Sony also published the P+NPsub junction type Pinned Photodiode in the Frame Transfer CCD image sensor in Tokyo and New York Press Conferences in 1978. Hagiwara was invited at CCD79 for his work.

**SONY HAD Sensor 1975 was hinted by SONY PNP Bipolar Transistor Process Technology**  
**Conventional Static Phototransistor**      **Dynamic Phototransistor Operation**  
*( by John Northrup Shive , 1950 )*      *with lightly doped base region*  
**Sony original Hole Accumulation Diode (HAD)**



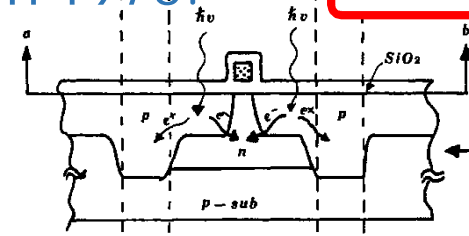
**Complete Charge Extraction from the N base region for low image lag and high speed high quality action pictures**

**See Japanese Patent 1975-134985**

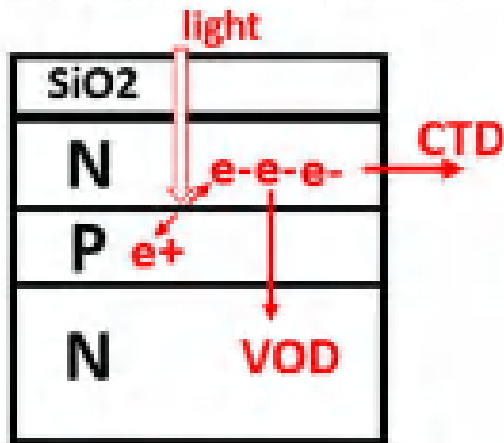
# Pinned Photodiode ( SONY original HAD Sensor ) was invented by Hagiwara at Sony in 1975.

SONY HAD is by necessity a Pinned Photodiode.  
A Pinned Photodiode is by necessity a Buried Photodiode.  
But not all Buried Photodiodes are pinned, and  
NEC Buried Photodiode is not by necessity a Pinned Photodiode.

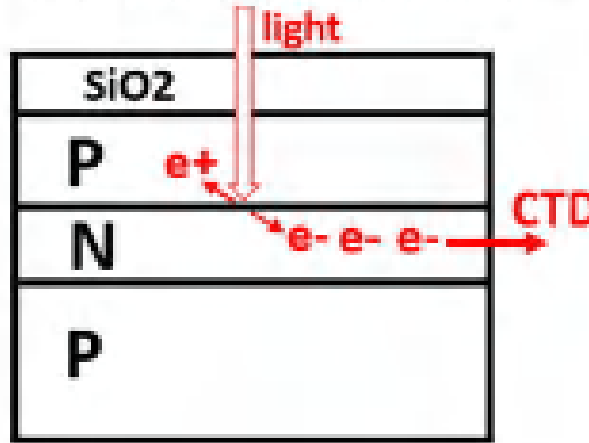
No Image Lag



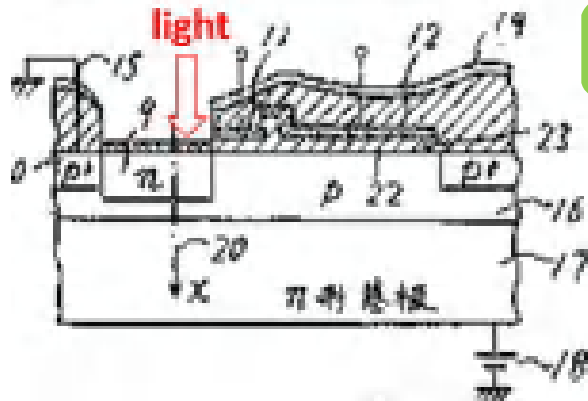
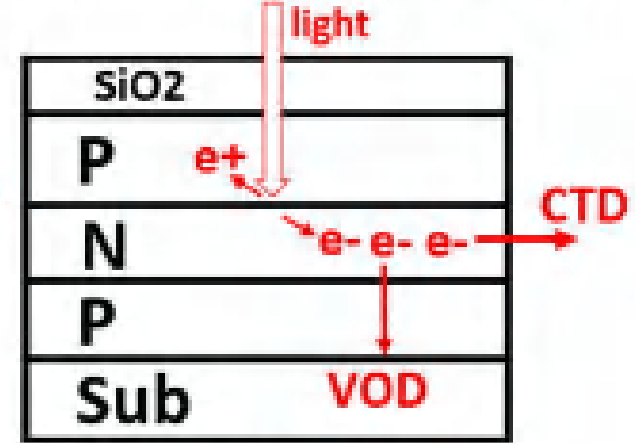
**Yamada 1978 at Toshiba**  
Japanese Patent 1978-1971  
NPN Junction Photodiode



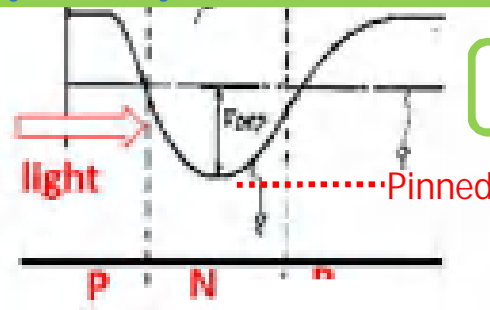
**Shiraki&Teranishi 1980 at NEC**  
Japanese Patent 1980- 123259  
PNP Junction Photodiode



**Hagiwara 1975 at Sony**  
Japanese Patent 1975-134985  
PNPSub Junction Photodiode

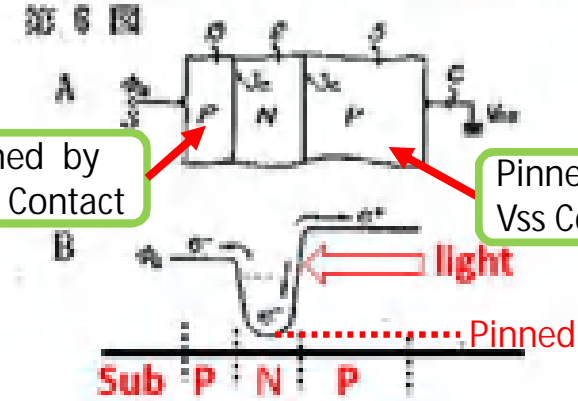


But, NEC Buried Photodiode is NOT by necessity a Pinned Photodiode.



Pinned by VOD Contact

Pinned by Vss Contact

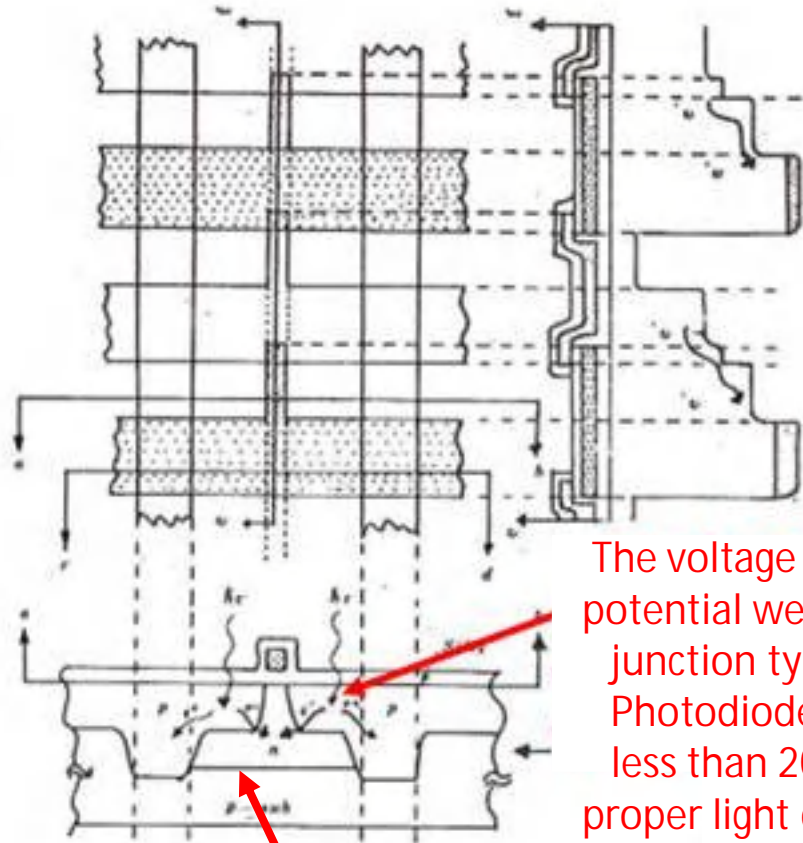




The first publication of a PNP junction type Pinned Photodiode in 1978 at Tokyo Conference

Proceeding of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Applied Physics, Volume 18(1979) Suuplement 18-1, pp.335-340 "A 388H x 488V CCD Imager with Narrow Channel Transfer Gate" reported by Yoshiaki Daimon-Hagiwara, Motoaki Abe and Chikao Okada

See JP 1975-134985



The voltage of the empty potential well of this PNP junction type Pinned Photodiode can be set less than 20 volts by a proper light doping level

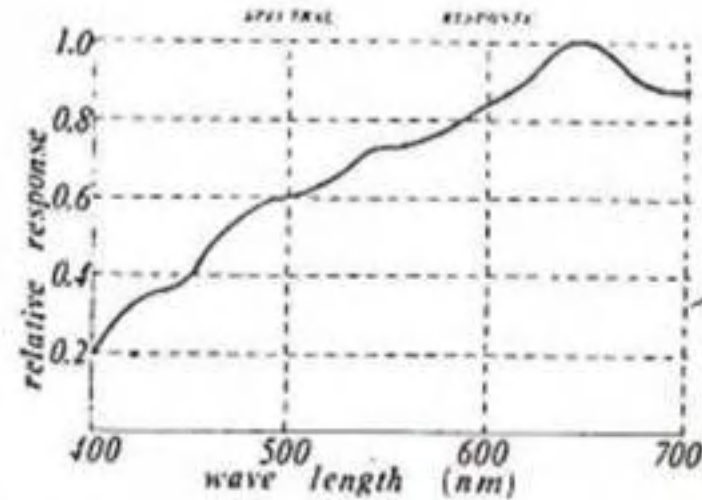
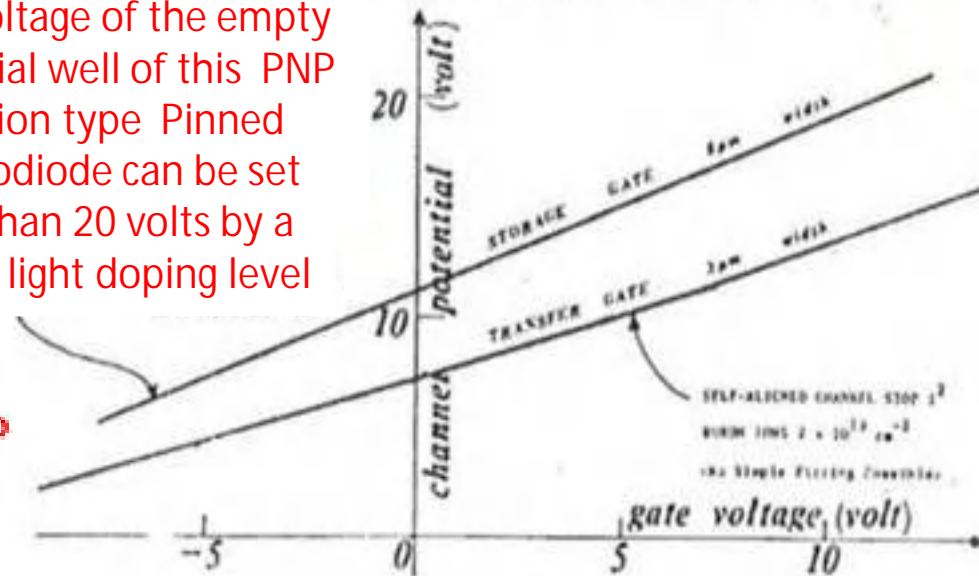


Fig. 18. Spectral Response of the photosensors.

The first publication of a PNP junction type Pinned Photodiode in 1978 at Tokyo, Japan by Hagiwara at Sony



# Pinned Photodiode Family Tree

Hagiwara is the inventor of the KODAK Pinned Photodiode, the NEC Buried Photodiode and the SONY HAD sensor.

**Grand Father**

Hagiwara Patent 1975-127647  
on the  $N+N_{sub}P+N$  junction  
Pinned/Buried Photodiode  
with Global Shutter Scheme  
and Back Light Illumination

**Grand Mather**

Hagiwara Patent 1975-134985  
on the  $P+NPN_{sub}$  junction  
Pinned Photodiode  
with Vertical OFD (VOD)

**MOTHER**

Hagiwara CSSD 1978 Paper  
of the  $P+NP_{sub}$  junction  
Pinned Photodiode  
on the 380H x 490V FT CCD Imager

**First Child**

NEC IEDM1982 Paper  
of the  $PNP_{sub}$  junction  
Buried Photodiode  
on the ILT CCD Imager

**Second Child**

KODAK IEDM1984 Paper  
of the  $P+NP_{sub}$  junction  
Pinned Photodiode  
on the MOS Imager

**Third Child**

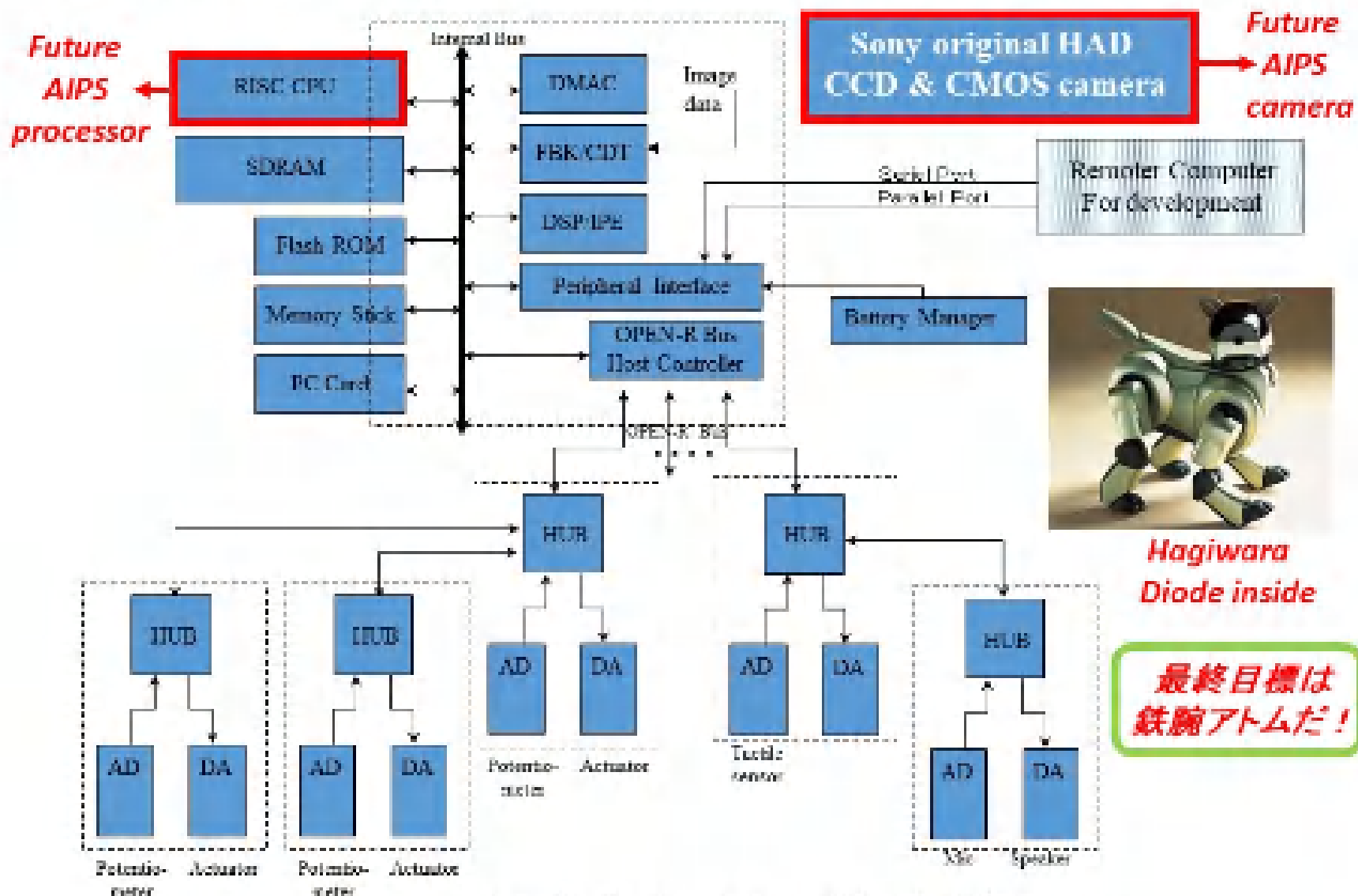
SONY 1987 HAD Sensor  
of the  $P+NP_{well}N_{sub}$  junction  
Pinned Photodiode  
with Vertical OFD (VOD)



Type	Classical N+Psub Photodiode	Surface Channel CCD Photodiode	Buried Channel CCD Photodiode	Toshiba 1978 NPNsub Photodiode	NEC 1980 PNP Buried Photodiode	SONY HAD Hagiwara 1975 P+NPNsub Pinned Photodiode
Blue Light Sensitivity	○	×	×	○	○	○
Image Lag	×	○	○	×	○	○
Surface Dark Current	×	×	×	×	×	○
Surface Trap Noise	×	×	○	×	×	○
Vertical OFD (VOD)	×	×	×	○	×	○
Global Shutter	×	○	○	×	×	○

Hagiwara at Sony filed two Japanese Patents in 1975. One ( JAP 1975-127647 ) is the N+NP+N junction type Pinned Photodiode with the MOS type CTG as **the Global Shutter Buffer Memory**. And the other (JAP 1975-134985) is the P+NPNsub junction type Pinned Photodiode with **the built-in vertical overflow drain (VOD)** and the hole accumulation surface P+ layer with the pinned surface potential. The P+ layer quenched the positively charged surface fixed trap states Qss that would create the serious surface dark current.

# SONY AIBO 2<sup>nd</sup> Generation, ERS-210



Logical Hardware Block Diagram