Pinned Photo Diode

Yoshiaki Hagiwara at Sony invented the Pinned Photo Diode in 1975.
Pinned Photo Diode is identical to SONY HAD (Hole Accumulation Diode).
Please Visit http://www.aiplab.com/

For the original document, visit and search the Japanese Official Patent Web:
https://www4.j-platpat.inpit.go.jp/eng/tokujitsu/tkbs_en/TKBS_EN_GM101_Top.action
Yoshiaki Hagiwara visited his friends in Sony Kumamoto Technology Center on November 19, 2018.
Pinned Photo Diode

Yoshiaki Hagiwara at Sony invented the Pinned Photo Diode in 1975. Pinned Photo Diode is identical to SONY HAD (Hole Accumulation Diode).

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For the original document, visit and search the Japanese Official Patent Web:
Empty Potential Well of Pinned Photo Diode

See JAP 1975-134985 and 1975-127647 drawn for the first time by Hagiwara at Sony in 1975

Microelectronics Journal
Volume 40, Issue 1, January 2009, Pages 137-140

The effect of size on photodiode pinch-off voltage for small pixel CMOS image sensors

Empty Potential Well of Pinned Photo Diode

See JAP 1975-134985 and 1975-127647 drawn for the first time by Hagiwara at Sony in 1975

"Quanta Image Sensor: Possible paradigm shift for the future "

by Eric R. Fossum March 22, 2012

"Grand Keynote",


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Charge storage in buried or pinned photodiode

- No Si-SiO₂ interfaces, low trapping and generation
- All silicon, well gettered, few defects
- Diffusion-limited dark current
- Complete charge transfer for readout
- "Large" structure, must store full well signal.

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Figure 6 of JAP 1975-134985

Figure 7 of JAP 1975-127647

Floating P+ region can be drained completely for image lag free mode
But after the 1978 Sony Press Conference in Tokyo and New York, where one chip FT CCD image sensor camera using the Pinned Photo Diode was announced, SONY was secretly preparing already for mass production as the company top secret. After the CCD79 presentation at Edinburgh, Scotland UK, Hagiwara was convincing the SONY TOP managements for the one chip IT image sensor using the Pinned Photo Diode that Hagiwara defined in his 1975 patents. See the Fig. 6 of JAP 1975-134985 and the Fig.7 of JAP 1975-127647 respectively. Hagiwara wishes that you all agree with Hagiwara that Hagiwara at Sony is the true inventor of the Pinned Photo Diode.

As Fossum himself defined in his presentation the empty potential well of the Pinned Photo Diode, you can see that it is identical to the empty potential well that Hagiwara at Sony drew in his patents in 1975. The Pinned Photo Diode is identical to the SONY HAD (Hole Accumulation Diode), too. A very few SONY people know this fact unfortunately.

Until June 2018, Hagiwara was not aware of what was going on in the image sensor community because Hagiwara was completely retired. After the ISSCC2013 plenary panel talk, Hagiwara retired completely. Hagiwara was happy with the last honorable presentation at the ISSCC2013 events. Hagiwara thought he could now retire completely. Hagiwara did not know what was going on in the last five years until in June 2018 Hagiwara found the Fossum 2014 FAKE paper.

Hagiwara feels very sorry for having induced a large noise and confused young generation engineers who are not aware of the true history of image sensor developments. The image sensor community and the IEEE EDS society made a lot of WRONG citations and narratives on the inventor of Pinned Photo Diode in the last five years after the 2014 Fossum FAKE paper.

The truth is that, the inventor of the Pinned Photo Diode is NOT Teranishi-san although he did a good job for developing a large scale IT CCD image sensor using the Pinned Photo Diode at NEC.

However, according to the official Japan Invention Web site, Teranishi-san is cited as the inventor of the pinned photo diode? Yamada-san at Toshiba is cited as the inventor of the Vertical Overflow Drain? And Suzuki-san at SONY is cited as the inventor of the back illumination image sensor? Hagiwara is puzzled and not happy on these citations and related public narratives.
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

Conventional Static Photo Transistor of PNP junction type

- Collector
- Emitter
- Photo Transistor Symbol

According to the light intensity, the collector current is modified in the conventional phototransistor.

Dynamic Photo Transistor Operation proposed by Hagiwara Sony in 1975

- Emitter
- Back Light
- Collector
- Front Light

The charge transfer device (CTD) can be CCD and/or CMOS type

The base photo generated charge is extracted to the adjacent CTD dynamically.

PNP/Sub junction type Pinned Photo Diode

CCD or CMOS Type Charge Transfer Device
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

with vertical overflow drain (VOD) function
including back light illumination scheme

A Pinned Photo Diode defined in the Patent Claims

Structure defined for Upside-Down Wafer

Back Light

V_{Sub} \rightarrow \text{Sub}

V_{OFD} \rightarrow \text{P}

J_e \rightarrow \text{N}

J_c \rightarrow \text{P}

V_{SS} \rightarrow \text{Pinned}

Front Light

Wafer Front Side

The basic P/N/P/Sub junction (thyristor) type Photo Sensor can have various kinds of Vertical Overflow Drain (VOD) functions.

This patent structure can include both the back and front light illumination schemes.

Sub can be N_{sub} or P_{sub}

CCD or CMOS Type Charge Transfer Device

Pinned V_{SS}
(1) In the semiconductor substrate (Sub)
(2) the first region (P) is formed,
(3) and the second region (N) is formed upon on the first region (P),
(4) forming the photo sensing part (NP).
(5) The charge from this (NP) is transferred to the charge transfer device (CTD),
(6) which is formed along the front surface of the semiconductor substrate (Sub).
(7) In the so-defined image sensing device,
(8) on the second region (N) of the photo sensing part (NP),
(9) a rectifying junction (PN) is formed.
(10) Let this junction (PN) be called an emitter junction (Je).
(11) Let the junction between the first region (N) and the second region (P)
(12) be called as the collector junction (Jc) forming a transistor (PNP).
(13) In the second region (N), which is the base of the said transistor (PNP),
(14) according to the optical image, the electronic charge (e-) is stored.
(15) The electronic charge (e-) stored in here (N), is transferred to the said CTD.
(16) The image sensor structure with such a charge transfer operation
(17) with the features explained above is in the scope of this patent claim.

This Japanese Patent 1975-134985 shown here is the evidence to claim that the Pinned Photo Diode with the vertical overflow drain (VOD) function was invented by Yoshiaki Daimon Hagiwara at Sony in 1975.
This patent structure can include both the front and back light illumination schemes.
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

Patent Claim in English Translation

Fig. 6

1. Along the main surface of the silicon substrate die (Sub),
2. the charge transfer gate (CTG) is formed upon the oxide layer (SiO2).
3. whereby the first region (N) is formed for charge transferring area (CTD).
4. On the other side of the silicon substrate die (Sub),
5. another region (P) is formed nearby the charge transferring area (CTD).
6. The region (P) and the nearby first region (N) together
7. form a photo sensing area (NPN junction).
8. By applying a proper pulse (P1) onto the charge transfer gate (CTG),
9. the charge (e+) stored in the photo sensing area (PNP junction) is transferred to the charge transfer area (CTD).
10. And upon the said transfer gate (CTG),
11. a different type of clock pulse (P2) is applied, which is different from the previous pulse (P1).
12. Along the main surface of the silicon substrate die (Sub)
13. the charge (e+) is transferred in this way.
14. And so defined solid state image sensor is in the scope of this patent claim.
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

The Pinned Photo Diode Structure defined in this Patent Claim

Fig.6

Patent Claim in Japanese  特許請求範囲

(1)半導体基体の一方の主面側に、
(2)絶縁膜を介して電荷転送用電極が配列される
(3)1の導電型の転送領域が形成され、
(4)之より上記半導体基体の他方の主面側に
(5)上記転送領域に接する他の導電型の領域と
(6)該領域に接する1の導電型の領域とより成る
(7)受光領域が形成され、
(8)上記転送用電極に所要の電圧を印加することにより、
(9)上記受光領域に蓄積した電荷を上記転送領域に転送し、
(10)上記電荷転送用電極に
(11)上記所要の電圧とは異なるクロック電圧を印加して
(12)上記基体の上記主面の主面に沿って
(13)電荷の転送を行うようにしたことを
(14)特微とする固体画像装置。
Patent Claim in English Translation

(1) Along the front surface of a semiconductor substrate (Nsub),
(2) the charge transfer gate (CTG) is placed upon the oxide,
(3) whereby a first region (P) is formed for charge transfer
(4) On the opposite side of this region (P),
(5) on the back side of the semiconductor substrate (Nsub),
(6) in between the region (P) for charge transfer,
(7) a base region (N) of another doping is formed.
(8) Nearby, a photo sensing region (P) is formed.
(9) By applying a proper voltage (Vbase) to the base region (N),
(10) The electronic charge (e+) which is stored in the photo sensing region (P),
(11) is transferred to the charge transfer region (P).
(12) By applying a proper clock pulse to the charge transfer gate (CTG),
(13) the charge is further transferred in the CTD.
(14) So defined solid state image sensor with the features described above is in the scope of the patent claim.

Figure 7
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Patent Claim in English

(1) 半導体基体に一方の主面側に、
(2) 絶縁膜を介して電荷伝送用電極が配列される
(3) 1の導電型の転送領域が形成され、
(4) 之に対向し且つ之より
(5) 上記半導体基体の他方の主面側に
(6) 上記転送領域との間に
(7) 他の導電型のベース領域
(8) を介して受光領域が形成され、
(9) 上記ベース領域に所定電圧を印加することにより
(10) 上記受光領域に蓄積した電荷を
(11) 上記転送領域に転送し
(12) 上記電荷転送用電極に所定のクロック電圧を印加して
(13) 電荷の転送を行うようにしたことを
(14) 特徴とする固体撮像装置
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975
with vertical overflow drain (VOD) function including back light illumination scheme

File: 1975-134985  Filed: 1975/11/10
Public: 1975-058414  Public: 1977/05/13
Grant: 1983/10/19

A Pinned Photo Diode defined in the Patent Claims

The basic P/N/P/Sub junction (thyristor) type Photo Sensor can have various kinds of Vertical Overflow Drain (VOD) functions.

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer

CCD or CMOS Type Charge Transfer Devise

This patent structure can include both the back and front light illumination schemes.
The evidence that Hagiwara at Sony is the inventor of the pinned photo diode.

See Fig.6 of Y. Hagiwara, Japanese Patent App 50 - 134985,

Conventional Buried Channel CCD
empty potential well

Pinned Photo Diode (Hagiwara 1975 invention)
empty potential well

Metal oxide semiconductor

Buried Channel Type CCD MOS capacitance

PNP junction transistor capacitance

Fig.6

Hagiwara Diode
1975 Photo Sensor,
Good sensitivity,
No Image Lag,
Built-in VOD,
Low dark current
And Low Noise.

In 1975, Hagiwara
drew for the first
time in the world
the empty potential
well curve in Pinned
Photo Diode.

Hagiwara in 1975 drew
an empty potential well
in the empty base
N storage layer
of the dynamic PNP
transistor capacitance
for the first time
in the world in 1975.

CCD type light sensing structure has poor light sensitivity.
### Comparison of four types of Light Detecting Sensor Structures

<table>
<thead>
<tr>
<th>Feature</th>
<th>N+P&lt;sub&gt;sub&lt;/sub&gt;</th>
<th>SCCD</th>
<th>BCCD</th>
<th>P+N-PN&lt;sub&gt;sub&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity</td>
<td>O</td>
<td>X</td>
<td>X</td>
<td>O</td>
</tr>
<tr>
<td>Image Lag</td>
<td>X</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>Surface Dark Current</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>O</td>
</tr>
<tr>
<td>Surface Trap Noise</td>
<td>X</td>
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<td>O</td>
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<tr>
<td>Vertical OFD Function</td>
<td>X</td>
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<td>X</td>
<td>O</td>
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<tr>
<td>Global Shutter Function</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
</tbody>
</table>

Hagiwara invented the P+N-PN<sub>sub</sub> type Pinned Photo Diode

See Japanese Patents (JA 1975-127647) and (JA 1975-134985)

The Pinned Photo Diode is much better than the CCD type light detector. The Active Pixell CMOS type DIGITAL CTD is much better than the CCD type ANALOG CTD.

In the total performance, CMOS Image sensor in digital system is considered to be much better than CCD image sensor in analog charge transfer system now.
In 1970s, we could not put the active source follower amplifier circuits in each small pixel. Image sensor engineers all knew that we had to wait until MOS process scaling down gets farther down. Until then, we needed the CCD type charge transfer device as the Super Star.
Engineers in 1966 working on the classical MOS image sensors already knew the conventional Source Follower Type Active Picture Element Cell (Pixell) Photo Diode, by the analogy of DRAM cases as shown above. Nothing is new about the Active Picture Element Cell (Pixell) Photo Diode CMOS image sensor.
This is a fake paper.

These (1) thru (9) statements are all biased and false. Many corrections are requested. Fossum is insulting Hagiwara and SONY by making many false statements.

This is the most serious false statement.

Yes, Hagiwara 1975 addressed the Complete Charge Transfer and Image Lag and anti-blooming, by drawings of Fig.5 and Fig.6 in Hagiwara 1975 patent on the original pinned photo diode.

Evidently, Fossum has never seen Hagiwara 1975 patent. In Fossum 2014 biased fake paper, Fossum did not quote the Fig.5 and Fig.6 of 1975 Hagiwara Patent invention.

This Fossum 2014 paper is a fake paper, insulting Hagiwara and Sony.

Fossum 2014 fake paper claims that 1982 Teranishi IEDM paper was the origin of the pinned photo diode which is not true. Fossum did not understand the physics of image sensors at all. He is a fake.
Origin of no-image-lag pinned photo diode invented by Hagiwara at SONY in 1975

High-Density and High-Quality Frame Transfer
CCD Imager with Very Low Smear, Low Dark
Current, and Very High Blue Sensitivity

Yoshiaki Hagiwara, Member, IEEE

(1) an ITL CCD imager application, (2) SONY 1978 FT CCD imager application (3) Heneczek 1979 invention
an example case shown in 1975 patent with original pinned photo diode of virtual phase CCD imager

(1) 1975 pinned photo diode sensor (2) 1978 pinned photo diode sensor (3) 1979 pinned photo diode sensor

Fig. 9. Three image sensors, Hagiwara 1975/1978, and Heneczek 1979, are compared. The boxed regions in the three sensors operate in the same charge transfer mechanism, which was later named by Heneczek, who applied this structure to realize, a virtual phase transfer CCD imager. The three sensors perform complete charge transfer. And no image lag is possible.


Teranish did not invent the pinned photo diode: Hagiwara at Sony did.

The pinned photo diode seen in Fossum 2014 paper, which is shown below, is the same as the SONY original HAD sensor invented by Yoshiaki Hagiwara at Sony in his 1975 patent.

**Hagiwara invented the pinned photo diode in 1975.**

Teranishi IEDM 1983 photo diode is a copy of Hagiwara 1975 invention

A Pinned Photo Diode of the P+N-PNsub junction (thyristor) type

with vertical overflow drain function invented by Hagiwara 1975


A Pinned Photo Diode defined in the Patent Claims
The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

One Schottky Barrier Image Sensor Application

One Pinned Photo Diode Image Sensor Application

Front Light

Charge Transfer Gate

SiO2

P+ N

P

Nsub

SiO2

Back Light

in case of Thinned Silicon Die

SONY HAD and PPD are the same thing!

PPD in Complete Charge Transfer Mode

Hole Accumulation Diode (HAD)

Buried Photo Diode

Vertical Charge Transfer from Buried Photo Diode

The Claimed Patent Structure does not include the metal contact on the top.
P+NPNsub junction (Thyristor) Type Photo Sensing Structure invented by Hagiwara in 1975 for the built-in vertical overflow drain (VOD) function and excellent blue light sensitivity with no image lag.

Pinned Photo Diode (PPD) and Sony original Hole Accumulation Diode (HAD), patented by Hagiwara at SONY in 1975 Japanese Patent (JAP 50-134985), originally defined as a dynamic photo sensing P+NPNsub junction Structure with the storage electron charge in the base N region to be transferred completely, from the N charge storage region in complete majority-carrier depletion mode, to the adjacent charge transfer device (CTD) to realize no image lag pictures.

The adjacent CTD can be historically a simple classical MOS image sensor, Bucket Brigade(BBD) type image sensor, Frame Transfer type CCD imager, Interline Transfer type CCD imager, or current CMOS technology active image sensor.

PPD and Sony HAD are the same thing, both invented by Hagiwara at Sony in 1975.
Hagiwara at Sony invented the pinned photo diode 1975.
See the JAPANESE PATENT, JAP 50-134985, 1975.

(1) Buried Channel CCD type
MOS capacitor sensor proposed in 1969

(2) Dynamic N-/P junction photo sensor conceived by Hagiwara 1975

Pinned Photo Diode (3) and (4) invented by Hagiwara 1975

(3) Dynamic P+/N-/P junction photo sensor invented by Hagiwara in 1975
(4) Dynamic P+/N-/P/Nsub junction photo sensor invented by Hagiwara in 1975

The key idea is lightly doped N-type storage layer in the pinned photo diode (3) and (4), for complete charge transfer with no image lag, similar to the lightly doped N-type buried layer of BCCD of type(1).

Reference: IEEE Solid-STATE CIRCUITS MAGAZINE, SUMMER 2013 issue, pp. 6
128-Bit Multicomparator

CARVER A. MEAD, RICHARD D. FLATBUSH, KOMURA, LEE D. BRITTAIN, YOSHIMI T. DAIMON, AND STEPHAN F. SANDO, JR., MEMBER, IEEE

Abstract-A 128-bit multicomparator was designed to perform the search-in-a database on accuracy limited data range. Device can be used as a large block length or modified for its panel, word, and bit applications. The circuit utilizes a large semi-dense shift register cell for data handling and a unique method to scan out data to accomplish the same function. The comparator is designed for high speed and uses two "input" registers with a 1:2:4:8:16 binary-to-analog convertor and a 1:2:4:8:16 encoder as the main elements of the comparator.

The multicomparator is fabricated using a circuit technology of solid-state monolithic (SSM) technology on a 0.1μm x 0.1μm chip contouring 160 pins. With standard-computing logic (SCC) gates, some area in terms of 2 bits have been printed. The entire power dissipation was 120 mW in the dynamic mode and 100 mW in the static mode.

Introduction

Over the past several years, there have been significant advances in the fabrication of large and complex semiconductor memories and conventional computer processing units (CPUs) is chip form. In the process, many other applications of large-scale integration (LSI) to computer architecture have been investigated [1]. LSI has now moved the technological distinction between logic and memory so that the two are now formally compatible. The CPU of a computer is replaced with a high-performance computer integrated circuit to improve system efficiency.

In this paper, a circuit diagram of a 128-bit multicomparator is described. The circuit consists of three independent independently studied dynamic-digital shift registers with associated exclusive-or gates. In operation, the device indicates a match between the data in the registers. The word in the key register is shifted into the key register and selecting the register in which the match occurs. While the word is being loaded, the comparator is enabled by an external signal.

1. Glossary


Ref: IEEE Journal of Solid State Circuits, VOl.SC11, No. 4, October 1976
Hagiwara was working on the buried channel type CCD charge transfer analysis, using IBM360 computers for his device simulation, which was published in ISSCC1974 in Philadelphia.

Charge-Coupled Devices and Applications

Chairman
Lewis M. Terman

My PhD thesis paper on buried channel CCD at ISSCC1974, in Philadelphia, USA

Prof. T. C. McGill

Prof. C. A. Mead
Prof. T. C. McGill

Prof. James McCaldin
AIPS digital circuits with two brains

L- Actuators
R- Actuators

Action Processor
Memory
Center Processor
Left Brain
Right Brain

Sensors

(1) Pinned Photo Diode
(2) Charge Transfer Device

AIPS BOX
The Japanese Patent 1975-134985 shown above is the evidence to claim that the Pinned Photo Diode with the vertical overflow drain (VOD) function was invented by Yoshiaki Hagiwara. Moreover, the Japanese Patent 1975-127647 shown above is the evidence to claim also that the Pinned Photo Diode with the back light illumination scheme was also invented by Yoshiaki Hagiwara at Sony in 1975.

Yoshiaki Hagiwara, the inventor of Pinned Photo Diode