Yoshiaki Hagiwara at Sony invented the Pinned Photo Diode in 1975. Pinned Photo Diode is identical to SONY HAD (Hole Accumulation Diode).

Please Visit http://www.aiplab.com/

For the original document, visit and search the Japanese Official Patent Web:
Yoshiaki Hagiwara visited his friends in Sony Kumamoto Technology Center on November 19, 2018.
Pinned Photo Diode

Yoshiaki Hagiwara at Sony invented the Pinned Photo Diode in 1975. Pinned Photo Diode is identical to SONY HAD (Hole Accumulation Diode).

Please visit http://www.aiplab.com/

Empty Potential Well of Pinned Photo Diode
See JAP 1975-134985 and 1975-127647 drawn for the first time by Hagiwara at Sony in 1975

Microelectronics Journal
Volume 40, Issue 1, January 2009, Pages 137-140

The effect of size on photodiode pinch-off voltage for small pixel CMOS image sensors

Empty Potential Well of Pinned Photo Diode

See JAP 1975-134985 and 1975-127647 drawn for the first time by Hagiwara at Sony in 1975

"Quanta Image Sensor: Possible paradigm shift for the future “
by Eric R. Fossum March 22, 2012

"Grand Keynote",

Charge storage in buried or pinned photodiode

- No Si-SiO₂ interfaces, low trapping and generation
- All silicon, well gettered, few defects
- Diffusion-limited dark current
- Complete charge transfer for readout
- “Large” structure, must store full well signal.
But after the 1978 Sony Press Conference in Tokyo and New York, where one chip FT CCD image sensor camera using the Pinned Photo Diode was announced, SONY was secretly preparing already for mass production as the company top secret. After the CCD79 presentation at Edinburgh, Scotland UK, Hagiwara was convincing the SONY TOP managements for the one chip IT image sensor using the Pinned Photo Diode that Hagiwara defined in his 1975 patents. See the Fig. 6 of JAP 1975-134985 and the Fig.7 of JAP 1975-127647 respectively. Hagiwara wishes that you all agree with Hagiwara that Hagiwara at Sony is the true inventor of the Pinned Photo Diode.

As Fossum himself defined in his presentation the empty potential well of the Pinned Photo Diode, you can see that it is identical to the empty potential well that Hagiwara at Sony drew in his patents in 1975. The Pinned Photo Diode is identical to the SONY HAD (Hole Accumulation Diode), too. A very few SONY people know this fact unfortunately.

Until June 2018, Hagiwara was not aware of what was going on in the image sensor community because Hagiwara was completely retired. After the ISSCC2013 plenary panel talk, Hagiwara retired completely. Hagiwara was happy with the last honorable presentation at the ISSCC2013 events. Hagiwara thought he could now retire completely. Hagiwara did not know what was going on in the last five years until in June 2018 Hagiwara found the Fossum 2014 FAKE paper.

Hagiwara feels very sorry for having induced a large noise and confused young generation engineers who are not aware of the true history of image sensor developments. The image sensor community and the IEEE EDS society made a lot of WRONG citations and narratives on the inventor of Pinned Photo Diode in the last five years after the 2014 Fossum FAKE paper.

The truth is that, the inventor of the Pinned Photo Diode is NOT Teranishi-san although he did a good job for developing a large scale IT CCD image sensor using the Pinned Photo Diode at NEC. But after the 1978 Sony Press Conference in Tokyo and New York, where one chip FT CCD image sensor camera using the Pinned Photo Diode was announced, SONY was secretly preparing already for mass production as the company top secret. After the CCD79 presentation at Edinburgh, Scotland UK, Hagiwara was convincing the SONY TOP managements for the one chip IT image sensor using the Pinned Photo Diode that Hagiwara defined in his 1975 patents. See the Fig. 6 of JAP 1975-134985 and the Fig.7 of JAP 1975-127647 respectively. Hagiwara wishes that you all agree with Hagiwara that Hagiwara at Sony is the true inventor of the Pinned Photo Diode.

As a visiting professor at Caltech in 1998 to 1999, when Hagiwara was teaching graduate students in Applied Physics and Electrical Engineering Departments, Hagiwara visited frequently JPL at Caltech, and met many diligent engineers at JPL, including Dr. Pain, who were working on the Active Pixel CMOS image sensors, while SONY was enjoying a big business on CCD image sensors at that time. The CMOS image sensor was NOT developed by Fossum alone. CMOS image sensors were developed by many people, including Sony engineers. Hagiwara himself alone did not develop the large scale image sensor either. Many young and clever, diligent and silent, Sony engineers also worked hard with back light illumination technology.

Hagiwara just invented the Pinned Photo Diode which is identical to SONY HAD sensor. Hagiwara believes also that Hagiwara himself invented the back light illuminated Pinned Photo Diode with the vertical Overflow Drain (VOD). See the two Japanese Patent by Hagiwara at Sony in 1975, JAP 1975-134985 and JAP 1975-127647.

The official Japan Invention Web site, Teranishi-san is cited as the inventor of the pinned photo diode?? Yammada-san at Toshiba is cited as the inventor of the Vertical Overflow Drain?? And Suzuki-san at SONY is cited as the inventor of the back illumination image sensor?? Hagiwara is puzzled and not happy on these citations and related public narratives.
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

Conventional Static Photo Transistor of PNP junction type

According to the light intensity, the collector current is modified in the conventional phototransistor.

Dynamic Photo Transistor Operation proposed by Hagiwara Sony in 1975

The charge transfer device (CTD) can be CCD and/or CMOS type

The base photo generated charge is extracted to the adjacent CTD dynamically.

Image Lag Free Complete majority Carrier charge Extraction From the base(N) region is possible.

PNP/Sub junction type Pinned Photo Diode
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975
with vertical overflow drain (VOD) function
including back light illumination scheme

A Pinned Photo Diode defined in the Patent Claims
Structure defined for Upside-Down Wafer

Back Light

Sub can be Nsub or Psub

Front Light

The basic P/N/P/Sub junction (thyristor) type Photo Sensor can have various kinds of Vertical Overflow Drain (VOD) functions.

This patent structure can include both the back and front light illumination schemes.

Basic Sensor Structure defined in this Patent

Fig. 6

Fig. 4

Example of VOD Schottky Barrier type Photo Diode in IT CCD sensor Application

Fig. 5

Example of VOD P+NSub Junction type Photo Diode in IT CCD sensor Application
In the semiconductor substrate (Sub) the first region (P) is formed, and the second region (N) is formed upon the first region (P), forming the photo sensing part (NP). The charge from this (NP) is transferred to the charge transfer device (CTD), which is formed along the front surface of the semiconductor substrate (Sub). In the so-defined image sensing device, on the second region (N) of the photo sensing part (NP), a rectifying junction (PN) is formed. Let this junction (PN) be called an emitter junction (Je). Let the junction between the first region (N) and the second region (P) be called as the collector junction (Jc) forming a transistor (PNP). In the second region (N), which is the base of the said transistor (PNP), according to the optical image, the electronic charge (e-) is stored. The electronic charge (e-), stored in here (N), is transferred to the said CTD. the image sensor structure with such a charge transfer operation with the features explained above is in the scope of this patent claim.

This Japanese Patent 1975-134985 shown here is the evidence to claim that the Pinned Photo Diode with the vertical overflow drain (VOD) function was invented by Yoshiaki Daimon Hagiwara at Sony in 1975.
This patent structure can include both the front and back light illumination schemes.
Pinned Photo Diode (NPN/Sub junction type)

The Pinned Photo Diode Structure defined in this Patent Claim

1. Along the main surface of the silicon substrate die (Sub),
2. the charge transfer gate (CTG) is formed upon the oxide layer (SiO2).
3. whereby the first region (N) is formed for charge transferring area (CTD).
4. On the other side of the silicon substrate die (Sub),
5. another region (P) is formed nearby the charge transferring area (CTD).
6. The region (P) and the nearby first region (N) together
7. form a photo sensing area (NPN junction).
8. By applying a proper pulse (P1) onto the charge transfer gate (CTG),
9. the charge (e+) stored in the photo sensing area (PNP junction) is transferred to the charge transfer area (CTD).
10. And upon the said transfer gate (CTG),
11. a different type of clock pulse (P2) is applied, which is different from the previous pulse (P1).
12. Along the main surface of the silicon substrate die (Sub)
13. the charge (e+) is transferred in this way.
14. And so defined solid state image sensor is in the scope of this patent claim.

Fig.6

Patent Claim in English Translation
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

The Pinned Photo Diode Structure defined in this Patent Claim

Patent Claim in Japanese

(1)半導体基体の一方の主面側に、
(2)絶縁層を介して電荷転送用電極が被着配列される
(3)１の導電型の転送領域が形成され、
(4)之より上記半導体基体の他方の主面側に
(5)上記転送領域に接する他の導電型の領域と
(6)該領域に接する１の導電型の領域とより成る
(7)受光領域が形成され、
(8)上記転送用電極に所要の電圧を印加することにより、
(9)上記受光領域に蓄積した電荷を上記転送領域に転送し、
(10)上記電荷転送用電極に
(11)上記所要の電圧とは異なるクロック電圧を印加して
(12)上記基体の上記一方の主面に沿って
(13)電荷の転送を行うようにしたことを
(14)特許とする固体像装置。
Pinned Photo Diode (NPN/Sub junction type)


Patent Claim in English Translation

(1) Along the front surface of a semiconductor substrate (Nsub),
(2) the charge transfer gate (CTG) is placed upon the oxide,
(3) whereby a first region (P) is formed for charge transfer
(4) On the opposite side of this region (P),
(5) on the back side of the semiconductor substrate (Nsub),
(6) in between the region (P) for charge transfer,
(7) a base region (N) of another doping is formed.
(8) Nearby, a photo sensing region (P) is formed.
(9) By applying a proper voltage (Vbase) to the base region (N),
(10) The electronic charge (e+) which is stored in the photo sensing region (P),
(11) is transferred to the charge transfer region (P).
(12) By applying a proper clock pulse to the charge transfer gate (CTG),
(13) the charge is further transferred in the CTD.
(14) So defined solid state image sensor with the features described above is in the scope of the patent claim.

Figure 7
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Patent Claim in English

(1) 半導体基体に一方の主面側に、
(2) 絶縁膜を介して電荷伝送用電極が配列される
(3) 1の導電型の転送領域が形成され、
(4) 之対向し且つ之により
(5) 上記半導体基体の他方の主面側に
(6) 上記転送領域との間
(7) 他の導電型のベース領域
(8) を介して受光領域が形成され、
(9) 上記ベース領域に所定電圧を印加することにより
(10) 上記受光領域に蓄積した電荷を
(11) 上記転送領域に転送し、
(12) 上記電荷転送用電極に所定のクロック電圧を印加して
(13) 電荷の転送を行うようにしたことを
(14) 特徴とする固体撮像装置

Fairchild Early Patent on CCD sensor with vertical OFD protection
USP3896485 (July 22, 1975)

Sony Hagiwara Patent on Pinned Photo Diode with P+NPNsub Thyristor type vertical OFD protection
JAP 1975-134985 (November 10, 1975)

Fairchild Early Patent, filed on July 22, 1975, applied on the surface CCD type MOS capacitance with poor blue sensitivity, while Sony Hagiwara Patent, filed on Nov. 10, 1975, applied on the Pinned Photo Diode, with good blue sensitivity and low dark current also with the built-in vertical overflow drain function, which was well known as the P+NPNsub Thyristor Punch-Thru action. Sony took more than ten years in this Patent War to challenge to explain the differences on the two image sensor structures and the two vertical overflow drain structures to the authorities who did not have any backgrounds on the semiconductor device physics.


1996年7月　日刊工業新聞記事から

(2000年1月米国最高裁で最終決着ソニー勝訴)

In January 2000, the US supreme court made the final judgement favoring Sony claims. And the long SONY-Fairchild Patent War on the PDD with the built-in vertical overflow drain (VOD) ended.
After the US court favored Sony over the SONY-Fairchild Patent War on the **Pinned Photo Diode**, Hagiwara received a thanking signature from Sony Chairman (Mr. Ohga), with many other official stamps from Sony executives including Sony President Idei, Sony Vice President Morio, Sony Top Executives Takahashi-san and Hori-san and others.

萩原が1975年発明したPinned Photo Diodeは、米国Fairchild社との特許戦争(1991-2000)に勝利し、またNEC社との特許戦争にも勝利し、SONY社内での評価も確立し、やっと萩原は特許収益を受けた。

Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975
with vertical overflow drain (VOD) function including back light illumination scheme

File 1975-134985 Filed 1975/11/10
Public 1975-058414 Public 1977/05/13
Grant 1983/10/19
A Pinned Photo Diode defined in the Patent Claims

The basic P/N/P/Sub junction (thyristor) type Photo Sensor can have various kinds of Vertical Overflow Drain (VOD) functions.

(a) Structure define for Up-Side Down wafer

Back Light

Sub can be Nsub or Psub

CTD

CCD or CMOS Type Charge Transfer Device

(b) Structure define for Up-Side Up wafer

Front Light

Wafer Front Side

CCD or CMOS Type Charge Transfer Device

Sub can be Nsub or Psub

This patent structure can include both the back and front light illumination schemes.
The evidence that Hagiwara at Sony is the inventor of the pinned photo diode.

See Fig.6 of Y. Hagiwara, Japanese Patent App 50 - 134985,

Conventional Buried Channel CCD
empty potential well

Pinned Photo Diode (Hagiwara 1975 invention)
empty potential well

Buried Channel Type CCD MOS capacitance

PNP junction transistor capacitance

Light is reflected by the metal gate

Light is reflected by the metal gate

Light is reflected by the metal gate

Light can go through the exposed SiO2 and reach the P+NP sub junction

Metal oxide semiconductor

Full Well

Empty Potential Well in the buried N layer of buried channel CCD

Flat Potential Well when electrons are in the buried N layer

Hagiwara Diode
1975 Photo Sensor,
Good sensitivity,
No Image Lag,
Built-in VOD,
Low dark current
And Low Noise.

In 1975, Hagiwara drew for the first time in the world the empty potential well curve in Pinned Photo Diode.

Hagiwara in 1975 drew an empty potential well in the empty base N storage layer of the dynamic PNP transistor capacitance for the first time in the world in 1975.

CCD type light sensing structure has poor light sensitivity
## Comparison of four types of Light Detecting Sensor Structures

<table>
<thead>
<tr>
<th>feature</th>
<th>N+P\textsubscript{sub}</th>
<th>SCCD</th>
<th>BCCD</th>
<th>P+N-PN\textsubscript{sub}</th>
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<tr>
<td>Sensitivity</td>
<td>O</td>
<td>X</td>
<td>X</td>
<td>O</td>
</tr>
<tr>
<td>Image Lag</td>
<td>X</td>
<td>O</td>
<td>O</td>
<td>O</td>
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<tr>
<td>Surface Dark Current</td>
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<td>X</td>
<td>O</td>
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<tr>
<td>Surface Trap Noise</td>
<td>X</td>
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<td>O</td>
<td>O</td>
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<tr>
<td>Vertical OFD Function</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>O</td>
</tr>
<tr>
<td>Global Shutter Function</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
</tbody>
</table>

Hagiwara invented the P+N-PN\textsubscript{sub} type Pinned Photo Diode

See Japanese Patents (JA 1975-127647) and (JA 1975-134985)

The Pinned Photo Diode is much better than the CCD type light detector.
The Active Pixell CMOS type DIGITAL CTD is much better than the CCD type ANALOG CTD.

In the total performance, CMOS Image sensor in digital system is considered to be much better than CCD image sensor in analog charge transfer system now.
The original SONY HAD Sensor Patent

HAD = Hole Accumulation Diode

Abstract:

A solid state imager device having a charge accumulating region (P) of a second conductivity type (p-type) formed on the surface side of a semiconductor substrate (Nsub) of a first conductivity type (n-type) which has a charge accumulating region (P) of the second conductivity type (p-type) laminated on the charge accumulating region (N), the second conductivity type region (P) and the charge accumulating region (N) forming a charge accumulating section (PN junction), and a first conductivity type region (N) formed on the surface of and/or on the side of the second conductivity type region (P), wherein if an excessive signal charge is produced in the charge accumulating section (N), the excessive signal charge is absorbed in the first conductivity type region (Nsub), whereby brooming can be satisfactorily suppressed and higher integration of the device can be achieved.
USP 4851887 by Yoshiaki Hagiwara

Priority Date 1987-01-19

hinted by JAP 1975-134985

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view showing a main portion of an example of a previously proposed solid state imager device; with lateral OFD.

FIG. 2 is a cross-sectional view showing a main portion of another example of a previously proposed solid state imager device; with vertical OFD.

FIG. 3 is a cross-sectional view showing a main portion of an embodiment of a solid state imager device according to the present invention; with vertical OFD.

This Lightly doped N-/Psub Photo Diode was also a new idea of Hagiwara in 1975 shown in JAP 1975-134985, NOT patented.

One example of the P+N-P junction type Photo Diode with Vertical OFD

Figure 4 of JAP 1975-134985

See Fig. 1 and Fig. 2 above

Figure 6 of JAP 1975-134985

The P+NPNsub Pinned Photo Diode of JAP 1975-134985 includes the structures of Fig. 1 and Fig. 2 shown above.
Thus, brooming can be satisfactorily removed. According to the present embodiment, it is not necessary to provide the region, to which excessive signal charges are discharged, on the surface of the semiconductor substrate adjacent to the charge accumulating region as the lateral overflow-structured solid state imager device, so that a dimension or area per one pixel can be reduced, whereby high integration can be achieved. 

Also, in this invention it is not necessary to form on the N-type silicon substrate the P-type diffusion region which has difficulty in forming conditions, as the vertical overflow-structured solid state imager device, so that the manufacture thereof becomes more easily. The above-described embodiment is the case where the present invention is applied to an interline transfer solid state imager device. Apart from that, the present invention can be also applied to a MOS-type solid state imager device, wherein the same effects as described above can be achieved. The above description is given on a single preferred embodiment of the invention but it will be apparent that many modifications and variations could be effected by one skilled in the art without departing from the spirits or scope of the novel concepts of the invention so that the scope of the invention should be determined by the appended claim only.
In 1970s, we could not put the active source follower amplifier circuits in each small pixel. Image sensor engineers all knew that we had to wait until MOS process scaling down gets farther down. Until then, we needed the CCD type charge transfer device as the Super Star.
History of DRAM Cell

Conventional DRAM Cell before 1966

R.H. Dennard (IBM 1966)

Bill Regitz (Honeywell 1969)
Intel 1101 @ISSCC1970, Philadelphia.

History of Photo Diode Cell

Conventional Active Photo Diode Cell before 1966

After R.H. Dennard (IBM 1966)

After Bill Regitz (Honeywell 1969)
Intel 1101 @ISSCC1970, Philadelphia.

Engineers in 1966 working on the classical MOS image sensors already knew the conventional Source Follower Type Active Picture Element Cell (Pixell) Photo Diode, by the analogy of DRAM cases as shown above. Nothing is new about the Active Picture Element Cell (Pixell) Photo Diode CMOS image sensor.
In 1975, Hagiwara filed a patent application on bipolar structures for CCDs in which a pnp vertical structure was disclosed, among several structures [24]. The top p layer was connected by metal in a bias used to control full-well capacity and the n-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called “Hole Accumulation Diode” or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the “narrow-gate” CCD with an open p-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

Yes, Hagiwara 1975 addressed the Complete Charge Transfer and Image Lag and anti-blooming, by drawings of Fig.5 and Fig.6 in Hagiwara 1975 patent on the original pinned photo diode.

Evidently, Fossum has never seen Hagiwara 1975 patent. In Fossum 2014 biased fake paper, Fossum did not quote the Fig.5 and Fig.6 of 1975 Hagiwara Patent invention.
This Fossum 2014 paper is a fake paper, insulting Hagiwara and Sony.

Fossum 2014 fake paper claims that 1982 Teranishi IEDM paper was the origin of the pinned photo diode which is not true. Fossum did not understand the physics of image sensors at all. He is a fake.

Hagiwara Diode 1975

Fig. 5, Fig. 6A and Fig. 6B, shown as examples to explain the usefulness of the Japanese patent JP1215101 (JP58-46905) filed by Hagiwara at Sony in November 10, 1975.

Completely Image Lag Free
Origin of no-image-lag pinned photo diode invented by Hagiwara at SONY in 1975

High-Density and High-Quality Frame Transfer
CCD Imager with Very Low Smear, Low Dark
Current, and Very High Blue Sensitivity

Yoshiaki Hagiwara, Member, IEEE

(1) an ITL CCD imager application, an example case shown in 1975 patent
(2) SONY 1978 FT CCD imager application with original pinned photo diode
(3) Heneczek 1979 invention of virtual phase CCD imager

(1) 1975 pinned photo diode sensor (2) 1978 pinned photo diode sensor (3) 1979 pinned photo diode sensor

Fig. 9. Three image sensors, Hagiwara 1975/1978, and Heneczek 1979, are compared. The boxed regions in the three sensors operate in the same charge transfer mechanism, which was later named by Heneczek, who applied this structure to realize, a virtual phase transfer CCD imager. The three sensors perform complete charge transfer. And no image lag is possible.

Teranish did not invent the pinned photo diode: Hagiwara at Sony did.

The pinned photo diode seen in Fossum 2014 paper, which is shown below, is the same as the SONY original HAD sensor invented by Yoshiaki Hagiwara at Sony in his 1975 patent. Hagiwara invented the pinned photo diode in 1975.

A Pinned Photo Diode of the P+N-PNsub junction (thyristor) type with vertical overflow drain function invented by Hagiwara 1975


A Pinned Photo Diode defined in the Patent Claims
The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

Hole Accumulation Diode (HAD)
Front Light
SiO2
P+
N
P
Nsub
SiO2
Back Light
in case of Thinned Silicon Die

SONY HAD and PPD are the same thing!

PPD in Complete Charge Transfer Mode
Digital Output Scheme for PNP Junction Type Pinned Photo Diode with Back Light Illumination and Global Shutter

A New Application Example of PNP Junction Type Pinned Photo Diode

See the Japanese Patent (1975-134985) by Hagiwara 1975 at Sony.
Digital CMOS image sensor consisting of three basic blocks.

Block (1) Retina Nerve Cells (Hagiwara 1975 Retina Photo Diode)
Block (2) Charge Transfer Nerve Fibers (CMOS type digital CTD)
Block (3) Brain Memory Cells (Fast Cache SRAM and Slow NVRAM)

Digital CMOS image sensor

with highly sensitive and no image lag Hagiwara Diode (pinned photo diode)

We need also an AD convertor absolutely!!!

(1) Retina Nerve Cells
We don’t need CCD any more!
(2) Charge Transfer Nerve Fibers
(3) Brain Memory Cells

(1) Hagiwara 1975 Retina Diode (pinned photo diode)

But we still need Hagiwara Diode to achieve high sensitivity and no image lag.
Hagiwara 1975 Retina Diode (pinned photo diode)

Hagiwara diode, defined in Japanese Patent App 50 - 134985, 1975 and pinned photo diode are the same thing with the same structure.

Hagiwara diode invented by Hagiwara at Sony in his 1975 patent has the following five important features. They are (1) low CkT noise (2) low trap noise (3) low image lag and (4) good light sensitivity which are the same features of pinned photo diode, and more over (5) built-in VOD. The important features of (3) and (5) are shown by the empty potential well in his patent Fig.6B.

Hagiwara invented the pinned photo diode in 1975.

Yoshiaki (Daimon) Hagiwara
What is the Difference?

- Extended channel stop: two-phase (Sony) and light sensitivity (Philips), Hagiwara 1975 invention
  See JAP 1975-134985
- Pinned-photodiodes in CCD (NEC)
  Hagiwara 1975 invention
  See JAP 1975-127647
- Pinned-photodiodes in CMOS (Kodak)
  Sony original HAD and the PPD are the same thing, both are Hagiwara 1975 inventions.

The surface channel type CTD gate
See Hagiwara JAP 1975-127647

The buried channel type CTD gate
See Hagiwara JAP 1975-134985
Block (2) Charge Transfer Nerve Fibers (信号電荷転送用神経線)

Historically, CTD includes MOS type, BBD, CCD and CMOS type charge transfer devices.

CTD (charge transfer device); BBD (Bucket Brigade Device); CCD (charge coupled device);

CCD type CTD in 1970~2010

CMOS type CTD in 2010~present

We don’t need CCD any more!

Hagiwara invented the pinned photo diode in 1975.
IEDM1998 paper  (pp. 2.7.1-2.7.4)
A Snap-Shot CMOS Active Pixel Imager for Low-Noise, High-Speed Imaging

Guang Yang, Orly Yadid-Pecht, Chris Wrigley, and Bedabrata Pain
Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109, USA

Abstract
Design and performance of a 128x128 snap-shot imager implemented in a standard single-poly CMOS technology is presented. A new pixel design and clocking scheme allow the imager to provide high-quality images without motion artifacts at high shutter speeds (< 75 µsec. exposure), with low noise (< 5 e'), immeasurable image lag, and excellent blooming protection.

Introduction
Recent advances in CMOS imager technology have enabled the development of highly integrated, ultra-low power, camera-on-a-chip with impressive imaging performance [1, 2]. However, most CMOS imagers do not support simultaneous integration of all pixels in the imager, the imager being read out in a “rolling shutter” mode. Non-simultaneous exposure leads to image distortion whenever there is relative motion between the imager and the scene.

Fig. 1: Schematic of the snap-shot APS pixel. Hatched areas represent electrons.

Important Contribution to the Modern Digital CMOS Image Sensor Technology
A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads

FUMIO MIYAJI, YASUSHI MATSUYAMA, YOSHIKAZU KANAIISHI,
KATSUNORI SENOH, TAKASHI EMORI, AND
YOSHIKI HAGIWARA, MEMBER, IEEE

A 25-ns 4-Mbit CMOS SRAM with 512K word x 8-bit organization has been developed. The RAM was fabricated using a 0.5-μm poly and double-aluminum CMOS technology and was assembled in a 400-mil DIP. A small cell size of 3.6 × 5.875 μm² and a chip area of 46 × 17.41 mm² were obtained. A fast address access time of 25 ns using a single 3.3-V supply voltage has been achieved using our newly developed dynamic bit-line load (DBL) circuit scheme incorporated with an advanced transition detector (ATD), divided word-line structure (DWL), sense amplifier, and low-noise output circuit approach. A low operating current of 46 mA at 40 MHz and low standby currents of 70 μA (CMOS) were also attained.

I. INTRODUCTION

The MEMORY capacity of SRAM’s has quadrupled

See also Journal of the Solid State Circuits, Vol. 24, No.5, October 1989
Block (3) the brain nervous cells that store the image information.

**NVRAM** by Prof. S.M. Sze and **Cache SRAM** by Sony Hagiwara are original important digital media for handy digital cameras.

**ISSCC1989**

After the CCD work, Hagiwara and his team worked on the fast cache 25 nsec CMOS 4M bit SRAM silicon chip.

Important Contribution to the Modern Digital CMOS Image Sensor Technology
P+NPNsub junction (Thyristor) Type Photo Sensing Structure invented by Hagiwara in 1975 for the built-in vertical overflow drain (VOD) function and excellent blue light sensitivity with no image lag.

Pinned Photo Diode (PPD) and Sony original Hole Accumulation Diode (HAD), patented by Hagiwara at SONY in 1975 Japanese Patent (JAP 50-134985), originally defined as a dynamic photo sensing P+NPNsub junction Structure with the storage electron charge in the base N region to be transferred completely, from the N charge storage region in complete majority-carrier depletion mode, to the adjacent charge transfer device (CTD) to realize no image lag pictures.

The adjacent CTD can be historically a simple classical MOS image sensor, Bucket Brigade(BBD) type image sensor, Frame Transfer type CCD imager, Interline Transfer type CCD imager, or current CMOS technology active image sensor.

PPD and Sony HAD are the same thing, both invented by Hagiwara at Sony in 1975.
Hagiwara at Sony invented the pinned photo diode 1975.
See the JAPANESE PATENT, JAP 50-134985, 1975.

(1) Buried Channel CCD type
MOS capacitor sensor proposed in 1969

(2) Dynamic N-/P junction photo sensor conceived by Hagiwara 1975

(3) Dynamic P+/N-/P junction photo sensor invented by Hagiwara in 1975

(4) Dynamic P+/N-/P/Nsub junction photo sensor invented by Hagiwara in 1975

The key idea is lightly doped N-type storage layer in the pinned photo diode (3) and (4), for complete charge transfer with no image lag, similar to the lightly doped N-type buried layer of BCCD of type(1).

Reference: IEEE Solid-STATE CIRCUITS MAGAZINE, SUMMER 2013 issue, pp. 6
AIPS Digital CMOS image sensor consisting of three basic blocks.

Block (1) Retina Nerve Cells (Hagiwara 1975 Retina Photo Diode)
Block (2) Charge Transfer Nerve Fibers (CMOS type digital CTD)
Block (3) Brain Memory Cells (Fast Cache SRAM and Slow NVRAM)

AIPS digital circuits with two brains

L-Actuators
R-Actuators

(1) Pinned Photo Diode
(2) Charge Transfer Device

AIPS (Artificial Intelligent Partner System)

Yoshiaki (Daimon) Hagiwara
In 1978 for the first time in the world Sony published FT CCD image sensor with Hagiwara Photo Diode which was very highly light sensitive, with low noise and no image lag, which was the origin of the pinned photo diode as seen below.

But the world misunderstood that CCD imager is highly light sensitive. The truth is that Hagiwara Photo Diode is very highly light sensitive. Although CCD imagers had disappeared in the market, the Hagiwara Photo Diode (which is also called now as the pinned photo diode) is still active and working well in digital CMOS image sensors.

Hagiwara invented the pinned photo diode in 1975.
Hagiwara Diode, which is now called the pinned photo diode, was first introduced in CCD79 at University of Edinburgh, Scotland, UK.

**ADVANCES in CCD IMAGERS**

**ABSTRACT**

This paper provides a review of progress made in Sony on the technology and performance of CCD imagers for color video cameras. There are two basic approaches to realize a CCD image sensor, namely interline transfer organization and frame transfer organization. Sony has undertaken the design and fabrication of both types of the CCD imagers, and the development effort resulted in four different versions of CCD imagers. They are (1) a 240H x 490V interline transfer CCD image with high density structure, (2) signag-transfer CCD with checker-patte securing sites, (3) a 242H x 490V CCD image with SiO2 exposed photo-sensor arrays in frame transfer organization and (4) a 300H x 488V F.T. CCD im with narrow channel transfer gates. In this paper, the designs and operations of these CCD imagers and their camera systems are described in detail.

Hagiwara invented the pinned photo diode in 1975.
In 1980 SONY also announced the Two Chip ILT CCD image sensor.

Completely Image Lag Free CAMERA

Technical Report represented at Japan SSD conference Tokyo, May 1978

all solid state = robustness

透光電極(SnO2)露出型のMOS型受光構造を採用。その後高感度HAD構造を採用しソニーの1人勝ちとなるICX008

2/3 Inch 120K Pixcel IT CCD Imager designed
In 1984 SONY announced the SONY original HAD sensor, which is Hole Accumulation Photo Diode, another name for Hagiwara Diode 1975.

Origin of SONY HAD Sensor

Sony HAD (Hole Accumulation Diode) sensor is based on the dynamically operated P+NPNsub junction photo sensing structure invented by Yoshiaki Hagiwara and revealed in his patent in November 10, 1975.

EXview HAD CCD II

SonyのグローバルシャッターCCDによりカメラの感度を向上

SONY HAD Sensor and pinned photo diode are the same thing.

This P+NPNsub (HAD) sensor was also named later as the pinned photo diode because the accumulated majority carrier holes in P+ layer pins the P+ layer voltage.

Sonyは、光ダイオードの表面領域およびセンサーの感度を制御し、独自のマイクロレンズを組み込むサイドに設置して光をより多く集め、映像を合成することで、これを実現しています。

アプリケーション

- 影響度が製品の製造用のアプリケーション
- 一部の現状では特定のアプリケーション
- 特殊設定または製品の要件とする工場の自動化

PnP Image Sensor Structure proposed by Yoshiaki Hagiwara, 1975
See: JP3123305 (JP 59-449055)
After the CCD work, Hagiwara and his team worked on the fast cache 25 nsec CMOS 4M bit SRAM silicon chip with the dynamic bit line load for the first time in the world.

A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads

FUMIO MIYAJI, YASUSHI MATSUYAMA, YOSHIKAZU KANAISHI, KATSUNORI SENOH, TAKASHI EMORI, AND YOSHIKI HAGIWARA, MEMBER, IEEE

A 25-ns 4-Mbit CMOS SRAM with 512K word x 8-bit organization has been developed. The RAM was fabricated using a 0.8-μm single-poly and double-aluminum CMOS technology and was assembled in a 400-pin DIP. A small cell size of 3.6 × 5.875 μm² and a chip size of 74.6 × 17.41 mm² were obtained. A fast address access time of 25 ns and a single 3.3-V supply voltage has been achieved using our newly designed dynamic bit-line load (DBL) circuit scheme incorporated with an automatic transition detector (ATD), divided word-line structure (DWL), a sense amplifier, and low-noise output circuit approach. A low current of 46 mA at 40 MHz and low standby currents of 70 μA and 5 μA (CMOS) were also attained.

I. Introduction

The MEMORY capacity of SRAM's has quadrupled...
After the CCD work, Hagiwara and his team worked on the fast cache 25 nsec CMOS 4M bit SRAM silicon chip with the dynamic bit line load for the first time in the world.

Fig. 6. Concept of DBL.

ISSCC1989 paper
128-Bit Multicomparator

CARVER A. MEAD, RICHARD D. PASHLEY, NORMAN I., LEE D. BRITTEN, YOSHIWARI T. HAGIWARA, AND STEPHAN F. SANDO, JR., NINNAMA, NIB

Abstract - An n-bit multicomparator was designed to perform the search-function by the search-length, which can be used for selecting the most suitable device for a particular application. The circuit utilizes a single-stage circuit and requires only one decoder for a given set of n-bit comparisons. The circuit operates on a single-bit data word and is capable of comparing any two n-bit words.

INTRODUCTION

Over the past several years, there have been significant advances in the fabrication of large and fast semiconductor memories and conventional circuit layouts. The development of large-scale integration (LSI) technology has made it economically feasible to design the CPU of a computer by replacing much of its mainframe logic with LSI circuitry. This has led to an increased interest in improving system efficiency. Recently, an increasing number of products are being developed in this area, which are expected to be available in the near future. A great improvement in this direction can be made by developing peripheral logic units. This would allow each peripheral to accomplish its own internal processing and thus reduce CPU loading, thereby speeding up the overall system.

The circuit diagram of the multicomparator is shown in Fig. 1. The circuit consists of three independent stages, each of which is a dynamic shift register with a delay element between the stages. The delay elements are the latches that hold the data in the shift register until they can be latched onto the input word. The multicomparator is triggered by the presence of the input word in the shift register.

Fig. 1. Circuit diagram of multicomparator

Prof. C.A. Mead and Hagiwara (Daimon) at CalTech, Sept 1972.

128-Bit Multicomparator chip, designed by Hagiwara et al. and fabricated in Intel, 1972

Ref: IEEE Journal of Solid State Circuits, VOL. SC11, No. 4, October 1976
Hagiwara was working on the buried channel type CCD charge transfer analysis, using IBM360 computers for his device simulation, which was published in ISSCC1974 in Philadelphia.

Charge-Coupled Devices and Applications
Chairman
Lewis M. Terman

My PhD thesis paper on buried channel CCD at ISSCC1974, in Philadelphia, USA

Minimum Potential φ (volt)

Depth from Interface (Å)

Prof. T. C. McGill

Prof. C. A. Mead
Sensitivity
Cross-sectional photos

Front-illuminated CIS (without light guide)

Back-illuminated CIS

Back-illuminated CIS

Courtesy of Sony Corporation
Multi-functionality of Image Sensors

Pixels

ADC

3D integration technology connecting a pixel to an ADC

Requirements
- Advancement in three-dimensional LSI technology

Courtesy of Sony Corporation
SONY AIBO 2nd Generation, ERS-210

Future AIPS processor
- RISC CPU
- SDRAM
- Flash ROM
- Memory Stick
- PC Card

Internal Bus
- DMAC
- FBK/CDT
- DSP/LPE
- Peripheral Interface
- OPEN-R Bus Host Controller
- Battery Manager

Sony original HAD CCD & CMOS camera

Future AIPS camera

Remote Computer
For development

Hagiwara Diode inside

Logical Hardware Block Diagram

Courtesy of Sony Corporation
Pinned Photo Diode
invented by
Yoshiaki Hagiwara at Sony in 1975

Pinned Photo Diode is identical to SONY HAD (Hole Accumulation Diode)


As seen in Japanese Patent 1975-134985, Hagiwara at SONY is the inventor of the Pinned Photo Diode with the vertical overflow drain (VOD) structure.

Hagiwara at SONY is also the inventor of the Pinned Photo Diode with the back light illumination scheme as seen in Hagiwara 1975 Japanese Patent 1975-127647 and 1975-127646. The details are explained below.
Pinned Photo Diode

invented by
Yoshiaki Hagiwara at Sony in 1975

Pinned Photo Diode is identical to SONY HAD (Hole Accumulation Diode)

Visit https://www4.j-platpat.inpit.go.jp/eng/tokujitsu/tkbs_en/TKBS_EN_GM101_Top.action

and put the patent application number

1975-134985
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

Conventional Static Photo Transistor of PNP junction type

Dynamic Photo Transistor Operation proposed by Hagiwara Sony in 1975

According to the light intensity, the collector current is modified in the conventional phototransistor.

The base photo generated charge is extracted to the adjacent CTD dynamically.

PNP/Sub junction type Pinned Photo Diode
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975
with vertical overflow drain (VOD) function
including back light illumination scheme

A Pinned Photo Diode defined in the Patent Claims
Structure defined for Upside-Down Wafer

The basic P/N/P/Sub junction (thyristor) type Photo Sensor can have various kinds of Vertical Overflow Drain (VOD) functions.

This patent structure can include both the back and front light illumination schemes.
(1) In the semiconductor substrate (Sub)
(2) the first region ( P ) is formed,
(3) and the second region ( N ) is formed upon on the first region ( P ),
(4) forming the photo sensing part (NP).
(5) The charge from this (NP) is transferred to the charge transfer device (CTD),
(6) which is formed along the front surface of the semiconductor substrate (Sub).
(7) In the so-defined image sensing device,
(8) on the second region (N) of the photo sensing part (NP),
(9) a rectifying junction (PN) is formed.
(10) Let this junction(PN) be called an emitter junction (Je).
(11) Let the junction between the first region(N) and the second region (P)
(12) be called as the collector junction (Jc) forming a transistor (PNP).
(13) In the second region (N), which is the base of the said transistor (PNP),
(14) according to the optical image, the electronic charge (e-) is stored.
(15) The electronic charge (e-), stored in here (N), is transferred to the said CTD.
(16) the image sensor structure with such a charge transfer operation
(17) with the features explained above is in the scope of this patent claim.

This Japanese Patent 1975-134985 shown here is the evidence to claim that the Pinned Photo Diode with the vertical overflow drain (VOD) function was invented by Yoshiaki Daimon Hagiwara at Sony in 1975.
This patent structure can include both the front and back light illumination schemes.
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

(1) In the semiconductor substrate (Sub)

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

A Pinned Photo Diode defined in the Patent Claims

(2) the first region (P) is formed,

(2) 第1伝導型の第1半導体領域(P)と

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer
Pinned Photo Diode (PNP/Sub junction type)
See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

(3) and the second region (N) is formed upon on the first region (P),
(3) この上 (P) に形成された 第 2伝導型の 第 2半導体領域(N)
(a) Structure define for Up-Side Down wafer
(b) Structure define for Up-Side Up wafer
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

with vertical overflow drain function
invented by Hagiwara 1975

A Pinned Photo Diode defined in the Patent Claims

(4) forming the photo sensing part (NP).

(4) とが形成されて光感知部 (NP) と

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

(5) The charge from this (NP) is transferred to the charge transfer device (CTD).

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

with vertical overflow drain function
invented by Hagiwara 1975

File 1975-134985 Filed 1975/11/10
Public 1975-058414 Public 1977/05/13
Grant 1983/10/19

A Pinned Photo Diode defined in the Patent Claims

(6) which is formed along the front surface of the semiconductor substrate (Sub).

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer

Front Light

CTD

CCD or CMOS type Charge Transfer Device

Sub can be Nsub or Psub

Back Light

Sub

V_{Sub}

P

CTD

CCD or CMOS Type Charge Transfer Device

Wafer Front Side

Front Light

N

V_{Sub}

Sub

Back Light

V_{Sub}

P

N

Sub
Pinned Photo Diode (PNP/Sub junction type)
See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

In the so-defined image sensing device,

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer

Sub can be Nsub or Psub

CTD
CCD or CMOS type Charge Transfer Devise

Sub can be Nsub or Psub
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

A Pinned Photo Diode defined in the Patent Claims

(8) On the second region (N) of the photo sensing part (NP),

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer

CTD
CCD or CMOS type Charge Transfer Devise

Sub can be Nsub or Psub
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

A Pinned Photo Diode defined in the Patent Claims

(9) a rectifying junction (PN) is formed.

(a) Structure define for Up-Side Down wafer

Back Light

Sub

Sub can be Nsub or Psub

CTD

CCD or CMOS Type Charge Transfer Devise

Front Light

V_{OFD}

P

N

P

V_{Sub}

(b) Structure define for Up-Side Up wafer

Front Light

Wafer Front Side

CTD

CCD or CMOS Type Charge Transfer Devise

Sub can be Nsub or Psub

Back Light

Wafer Front Side

Sub

V_{OFD}

P

N

P

V_{Sub}
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

(10) Let this junction (PN) be called an emitter junction (Je).

(10) 該接合 (PN) をエミッタ接合 (Je) とし

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer

CTD
CCD or CMOS type Charge Transfer Device

Sub can be Nsub or Psub
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

with vertical overflow drain function
invented by Hagiwara 1975

A Pinned Photo Diode defined in the Patent Claims

(11) Let the junction between the first region (N) and the second region (P)

(11) 上記第 1(P)及び第 2半導体(N)間の接合を

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer

Front Light

V_{OFD}

Je

N

P

CTD

CCD or CMOS type Charge Transfer Devise

Back Light

V_{Sub}

Sub

Front Light

Wafer Front Side

Sub can be N_{sub} or P_{sub}

CTD

P

N

Wafer Front Side

CTD

CCD or CMOS type Charge Transfer Devise

Back Light

V_{Sub}

Sub

Front Light

Wafer Front Side

Sub can be N_{sub} or P_{sub}
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

(12) be called as the collector junction (Jc) forming a transistor (PNP),

(12) コレクター(Jc)とするトランジスタ(PNP)が形成し

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer

CTD

CCD or CMOS type Charge Transfer Device

Sub can be Nsub or Psub
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

A Pinned Photo Diode defined in the Patent Claims

(13) In the second region (N), which is the base of the said transistor (PNP),

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer

Sub can be Nsub or Psub
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

A Pinned Photo Diode defined in the Patent Claims

(14) according to the optical image, the electronic charge ($e^-$) is stored.

(14) 光学像に応じた電荷を蓄積し

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer
Pinned Photo Diode (PNP/Sub junction type)
See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

A Pinned Photo Diode defined in the Patent Claims

(15) The electronic charge (e-) stored in here (N) is transferred to the said CTD.
(15) ここに蓄積された電荷を
上記転送部(CTD)に移行させて、

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer
Pinned Photo Diode (PNP/Sub junction type)

See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

with vertical overflow drain function
invented by Hagiwara 1975

A Pinned Photo Diode defined in the Patent Claims

(16) the image sensor structure
with such a charge transfer operation

(16) その転送を行うようにしたことを

(a) Structure define for Up-Side Down wafer

(b) Structure define for Up-Side Up wafer
Pinned Photo Diode (PNP/Sub junction type)
See Japanese Patent 1975-134985 by Hagiwara at Sony in 1975

with vertical overflow drain function
invented by Hagiwara 1975

A Pinned Photo Diode defined in the Patent Claims

(17) with the features explained above
is in the scope of this patent claim.

(17) 特徴とする固体撮像装置

(a) Structure define for Up-Side Down wafer

Back Light

Sub

Sub can be Nsub or Psub

CTD

CCD or CMOS Type Charge Transfer Devise

Front Light

V_{Sub}

V_{OFD}

J_{e}

J_{c}

V_{Sub}

P

N

e-

e-

e-

(b) Structure define for Up-Side Up wafer

Wafer Front Side

CTD

CCD or CMOS type Charge Transfer Devise

Sub can be Nsub or Psub

V_{OFD}

J_{e}

J_{c}

V_{Sub}

P

N

e-

e-

e-

Front Light

Back Light
Pinned Photo Diode

invented by
Yoshiaki Hagiwara at Sony in 1975

Pinned Photo Diode is identical to SONY HAD (Hole Accumulation Diode)

Visit  https://www4.j-platpat.inpit.go.jp/eng/tokujitsu/tkbs_en/TKBS_EN_GM101_Top.action

and put the patent application number

1975-127647
These two Hagiwara 1975 Patents showed Empty Potential Wells of Completely-Majority-Carrier-Depleted Signal Charge Storage Areas implying Complete Charge Transfer Operations.
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

Visit https://www4.j-platpat.inpit.go.jp/eng/tokujitsu/tkbs_en/TKBS_EN_GM101_Top.action
And Input the Patent Application Number 1975-127647

The scope of the patent claims defines only the NPN Junction Type Pinned Photo Diode with the surface channel type charge transfer gate to the output CTD. This patent structure can also be applied to the large-area conventional ILT CCD image sensor.

The back light illumination scheme and the vertical overflow drain scheme are possible, optional as the patent application examples.

File 1975-127647  Filed 1975/10/23
Public 1975-051816  Public 1977/04/26

Fig. 6

Fig. 7

Pinned Photo Diode

Vertical OFD control (optional)

This array structure is also optional. This is also just one of the the patent application examples.

Floating P+ region can be drained completely for image lag free mode.
Pinned Photo Diode (NPN/Sub junction type)

The Pinned Photo Diode Structure defined in this Patent Claim

Fig. 6

Patent Claim in English Translation

(1) Along the main surface of the silicon substrate die (Sub),
(2) the charge transfer gate (CTG) is formed upon the oxide layer (SiO2).
(3) whereby the first region (N) is formed for charge transferring area (CTD).
(4) On the other side of the silicon substrate die (Sub),
(5) another region (P) is formed nearby the charge transferring area (CTD).
(6) The region (P) and the nearby first region (N) together
(7) form a photo sensing area (NPN junction).
(8) By applying a proper pulse (P1) onto the charge transfer gate (CTG),
(9) the charge (e+) stored in the photo sensing area (PNP junction) is transferred to the charge transfer area (CTD).
(10) And upon the said transfer gate (CTG),
(11) a different type of clock pulse (P2) is applied, which is different from the previous pulse (P1).
(12) Along the main surface of the silicon substrate die (Sub)
(13) the charge (e+) is transferred in this way.
(14) And so defined solid state image sensor is in the scope of this patent claim.
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

Fig. 6

The Pinned Photo Diode Structure defined in this Patent Claim

Patent Claim in Japanese

(1)半导体基体の一方の主面側に、
(2)絶縁膜を介して電荷輸送用電極が被着配列される
(3) 1の導電型の転送領域が形成される。
(4) 之より上記半導体基体の他方の主面側に
(5)上記転送領域に接する他の導電型の領域と
(6)該領域接する1の導電型の領域とより成る
(7)受光領域が形成される。
(8)上記転送用電極に所要の電圧を印加することにより、
(9)上記受光領域に蓄積した電荷を上記転送領域に転送し、
(10) 上記電荷転送用電極に
(11) 上記所要の電圧とは異なるクロック電圧を印加して
(12) 上記基体の上記一方の主面に沿って
(13) 電荷の転送を行うようにしたことを
(14) 特微とする固体映像装置。
Pinned Photo Diode (NPN/Sub junction type)
See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

(1) Along the front surface of a semiconductor substrate (Nsub),
(2) the charge transfer gate (CTG) is placed upon the oxide,
(3) whereby a first region (P) is formed for charge transfer

The Pinned Photo Diode Structure defined in this Patent Claim

![Diagram of Pinned Photo Diode](image-url)
Pinned Photo Diode (NPN/Sub junction type)
See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

(4) On the other side of the silicon substrate die (Sub),
(5) another region (P) is formed nearby the charge transferring area (CTD).

The Pinned Photo Diode Structure defined in this Patent Claim

Fig. 6
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

(6) The region (P) and the nearby first region (N) together
(7) form a photo sensing area (NPN junction).

The Pinned Photo Diode Structure defined in this Patent Claim

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975
By applying a proper pulse (P1) onto the charge transfer gate (CTG),

The Pinned Photo Diode Structure defined in this Patent Claim
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

(9) the charge (e+) stored in the photo sensing area (PNP junction) is transferred to the charge transfer area (CTD).

The Pinned Photo Diode Structure defined in this Patent Claim

(9) 上記受光領域に蓄積した電荷を上記転送領域に転送し、
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

(10) And upon the said transfer gate (CTG),
(11) a different type of clock pulse (P2) is applied, which is different from the previous pulse (P1).

The Pinned Photo Diode Structure defined in this Patent Claim
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127647 by Hagiwara at Sony in 1975

(12) Along the main surface of the silicon substrate die (Sub)
(13) the charge (e+) is transferred in this way.
(14) And so defined solid state image sensor
    is in the scope of this patent claim.

The Pinned Photo Diode Structure defined in this Patent Claim

The Pinned Photo Diode Structure is shown in the diagram on the right.

Fig. 6

A Pinned Photo Diode defined in the Patent Claim. The Scope of Patent Right is extended over all kinds of Operations and Usage of the structure.

PPD in Complete Charge Transfer Mode

SONY HAD and PPD are the same thing!
An application example of the P+P-NP junction type Pinned Photo Diode with Source follower type Active Current Amplifier and SNAP-SHOT capability. See Japanese Patent 1975-127647 (Hagiwara SONY 1975 invention).
Pinned Photo Diode (P+PNP junction type)

See JAP 1975-127647
Hagihara Sony 1975 Invention

The N- and N layer channel can be pinched off completely by the reverse voltage of the surrounding P/P+ layers, similar to the JFET operation.

Hinted by Pinched Off Junction Field Effect Transistor (JFET)

When the depletion layer is extended completely in the N-channel layer, the current can be cut-off to zero.

Current Off Mode
- \( V_G = 0 \) volt
- \( V_S = 1 \) volt
- \( V_D = 3 \) volt
- \( V_{sub} = 0 \) volt

Current On Mode
- \( V_G = 1 \) volt
- \( V_S = 1 \) volt
- \( V_D = 3 \) volt
- \( V_{sub} = 0 \) volt

Diffusion Current
\[ J = D \frac{dQ(x)}{dx} \]
Application of Narrow Channel and Channel Pinch Effects of Junction Filed Effect Transistor on the PNP junction type Pinned Photo Diode

Conventional Junction Field Effect Transistor

- $V_s$
- $V_d$
- $V_{th}$
- $N^+$
- $N^-$

- the channel is ON

PNP junction type Pinned Photo Diode

- $V_s$
- $V_d$
- $V_{th}$
- $N^+$
- $N^-$

- Back Light
- $e^-$

- the channel is OFF

Strong Punch-thru Voltage

- $V_s$
- $V_d$
- $V_{th}$

- $e^-$

Empty Well

- $V_s$
- $V_d$

- $e^-$

- Back Light

Analogue Data Comparator Chip

- Analog Data Comparator
- Analog Data Comparator

Top View of 2 x 2 pixel units

- Light

PNP Junction type Pinned Photo Diode

Hagiwara 1975 Invention
Digital Data Output Scheme for Pinned Photo Diode

Analog Data Comparator Chip

Analog Data Comparator

PNP Junction type Pinned Photo Diode
Hagiwara 1975 Invention

Top View of 2 x 2 pixel units

Light

Light

V_{PPD}(i,j)

V_{PD}

V_{PG}

V_{out}(i,j)

V_{Global Shutter}

T1

T2

T3

No Light

with Light on

No Light

with Light on

Signal Output

NPN Pre-charge Transistor

e^- @ t = T1

e+ @ t = T3

V_{sub}

Back Light

Comp\{i,j\}

V_{ref}

V_{SH}

V_{PG}

V_{dd}

V_{Global Shutter}

V_{out}(i,j)

V_{PD}

V_{PPD}(i,j)
7680 H x 4320 V image sensor

4320 V pixel units

SiO2

7680 H pixel units
Conventional Circuit

TOP DAC Chip

Memory Chips (1 ~ N)

One bit Memory Cell MC (i, j, k) Layout on the Kth Memory Floor Chip

Conventional Circuit

Analog Data Comparator Chip

Bottom Image Sensor Chip

Pinned Photo Diode Image Sensor with Back Illumination by Hagiwara 1975 invention

See Japanese Patent (1975-127647)
An application example of the P+P-NP junction type Pinned Photo Diode with Source follower type Active Current Amplifier and SNAP-SHOT capability. See Japanese Patent 1975-127647 (Hagiwara SONY 1975 invention).
Pinned Photo Diode

invented by
Yoshiaki Hagiwara at Sony in 1975

Pinned Photo Diode is identical to SONY HAD (Hole Accumulation Diode)

Visit https://www4.j-platpat.inpit.go.jp/eng/tokujitsu/tkbs_en/TKBS_EN_GM101_Top.action
and put the patent application number

JAP 1975-127646
An application example of the junction type Pinned Photo Diode with Source follower type Active Current Amplifier and SNAP-SHOT capability. See Japanese Patent 1975-127646 (Hagiwara SONY 1975 invention).
Back Light NP+N-N+ Junction Type Pinned Photo Diode
with the PP-N junction type buried channel type charge transfer gate

The Vertical PP-NP+ Junction type
Switching Pass Transistor
with the externally controllable base voltage

To CTD output

e+ (holes)

Switching Pass Transistor

NP+N- junction type
Pinned Photo Diode

Vertical OFD control

Buried Channel CCD type Charge Transfer Gates
transferring the holes (e+) to the adjacent CTD output.

Floating P+ Emitter can be drained completely.
Patent Claim in English Translation

(1) Along the front surface of a semiconductor substrate (Nsub),
(2) the charge transfer gate (CTG) is placed upon the oxide,
(3) whereby a first region (P) is formed for charge transfer
(4) On the opposite side of this region (P),
(5) on the back side of the semiconductor substrate (Nsub),
(6) in between the region (P) for charge transfer,
(7) a base region (N) of another doping is formed.
(8) Nearby, a photo sensing region (P) is formed.
(9) By applying a proper voltage (Vbase) to the base region (N),
(10) The electronic charge (e+) which is stored in the photo sensing region (P),
(11) is transferred to the charge transfer region (P).
(12) By applying a proper clock pulse to the charge transfer gate (CTG),
(13) the charge is further transferred in the CTD.
(14) So defined solid state image sensor with the features described above is in the scope of the patent claim.

Figure 7
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig. 6

特許請求範囲 Patent Claim in English

(1) 半導体基体に一方の主面側に、
(2) 絶縁膜を介して電荷伝送用電極が配列される
(3) 1の導電型の転送領域が形成され、
(4) 之に対向し且つ之より
(5) 上記半導体基体の他方の主面側に
(6) 上記転送領域との間に
(7) 他の導電型のベース領域
(8) を介して受光領域が形成され、
(9) 上記ベース領域に所定電圧を印加することにより
(10) 上記受光領域に蓄積した電荷を
(11) 上記転送領域に転送し
(12) 上記電荷転送用電極に所定のクロック電圧を印加して
(13) 電荷の転送を行うようにしたことを
(14) 特徴とする固体撮像装置
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig. 6

(1) Along the front surface of a semiconductor substrate (Nsub),

(1) 半導体基体に一方の主面側に
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig. 6

(2) the charge transfer gate (CTG) is placed upon the oxide,

(2) 绝縁膜を介して電荷伝送用電極が配列される

Fig. 7
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig. 6

Fig. 7

(3) whereby a first region (P) is formed for charge transfer

(3) 1の導電型の転送領域が形成される

CTD

CTG

SiO2

P

N_{sub}
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig. 6

Fig. 7

(4) On the opposite side of this region (P),

(4) 之に対向し且つ之より

<table>
<thead>
<tr>
<th>SiO2</th>
</tr>
</thead>
<tbody>
<tr>
<td>P</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>\text{N}_{\text{sub}}</td>
</tr>
</tbody>
</table>

File 1975-127646  Filed 1975/10/23
Public 1975-051815  Public 1977/04/26
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig. 6

(5) on the back side of the semiconductor substrate (N_{sub}),

Fig. 7

(5) 上記半導体基体の他方の主面側に

SiO2

P

N_{sub}
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

(6) in between the region (P) for charge transfer,

(6) 上記転送領域との間に

Fig.6

Fig.7

CTD

CTG

SiO2

P

N_{sub}
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig. 6

(7) a base region (N) of another doping is formed

(7) 他の導電型のベース領域

Fig. 7

<table>
<thead>
<tr>
<th>SiO2</th>
</tr>
</thead>
<tbody>
<tr>
<td>P</td>
</tr>
<tr>
<td>N</td>
</tr>
<tr>
<td>N_{sub}</td>
</tr>
</tbody>
</table>
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

(8) Nearby, a photo sensing region (P) is formed.

(8) erto shite saikō ni reikou ga seika sare,

Front Light  CTG

Back Light  CTD

<table>
<thead>
<tr>
<th>SiO2</th>
<th>P</th>
<th>N</th>
<th>P e+ e+ e+ e+</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>N_sub</td>
</tr>
</tbody>
</table>

Fig. 6

Fig. 7
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig.6

(9) By applying a proper voltage \( V_{\text{base}} \) to the base region \((N)\),

(9) 上記ベース領域に所定電圧を印加することにより

Front Light CTG

CTD

Back Light

Fig.7
Pinned Photo Diode (NPN/Sub junction type)
See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig.6

(10) The electronic charge (e+) which is stored in the photo sensing region (P),

Fig.7

(10) 上記受光領域に蓄積した電荷を
Pinned Photo Diode (NPN/Sub junction type)
See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig. 6

Fig. 7

(11) is transferred to the charge transfer region (P).
(11) 上記転送領域に転送し
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig. 6

(12) By applying a proper clock pulse to the charge transfer gate (CTG),

(12) 上記電荷転送用電極に所定のクロック電圧を印加して

Fig. 7
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

Fig. 6

Fig. 7

(13) the charge is further transferred in the CTD.

(13) 電荷の転送を行うようにしたことを
Pinned Photo Diode (NPN/Sub junction type)

See Japanese Patent 1975-127646 by Hagiwara at Sony in 1975

(14) So defined solid state image sensor with the features described above is in the scope of the patent claim.
An application example of the P-P-NPN junction type Pinned Photo Diode with Source follower type Active Current Amplifier and SNAP-SHOT capability. See Japanese Patent 1975-127646 (Hagiwara SONY 1975 invention).
Conventional Circuit

**TOP DAC Chip**

**Memory Chips (1 ~ N)**

**One bit Memory Cell MC (i, j, k) Layout on the Kth Memory Floor Chip**

**Conventional Circuit**

**Analogue Data Comparator Chip**

**Bottom Image Sensor Chip**

*Pinned Photo Diode Image Sensor with Back Illumination by Hagiwara 1975 invention*

*See Japanese Patent (1975-127647)*
AIPS digital circuits with two brains

- L- Actuators
- R- Actuators

(1) Pinned Photo Diode
(2) Charge Transfer Device
The Japanese Patent 1975-134985 shown above is the evidence to claim that the Pinned Photo Diode with the vertical overflow drain (VOD) function was invented by Yoshiaki Hagiwara. Moreover, the Japanese Patent 1975-127647 shown above is the evidence to claim also that the Pinned Photo Diode with the back light illumination scheme was also invented by Yoshiaki Hagiwara at Sony in 1975.